



MS-7693

CPU

VER:3.1

AMD M3 Phenom/Athlon 64 FX AM3/AM3R2

System Chipset

AMD RX980

ATI SB950

On Board Chip

FINTEK Super I/O -- F71878AD

LAN -- RTL8111EL

HD Codec --ALC887

ASM1042 USB3.0

BIOS -- SPI ROM 32M

Main Memory

DDR III X 4 (Max32GB)

Expansion Slots

PCI-E X 16*1

PCI-E X 4 *1

PCI-E X 1 *2

PCI 2.2 Slot X 2

PWM

Controller--IUPI1601 4+1 Phase

Vcore 4 Phase (MOS HIGHX2 LOWX2)

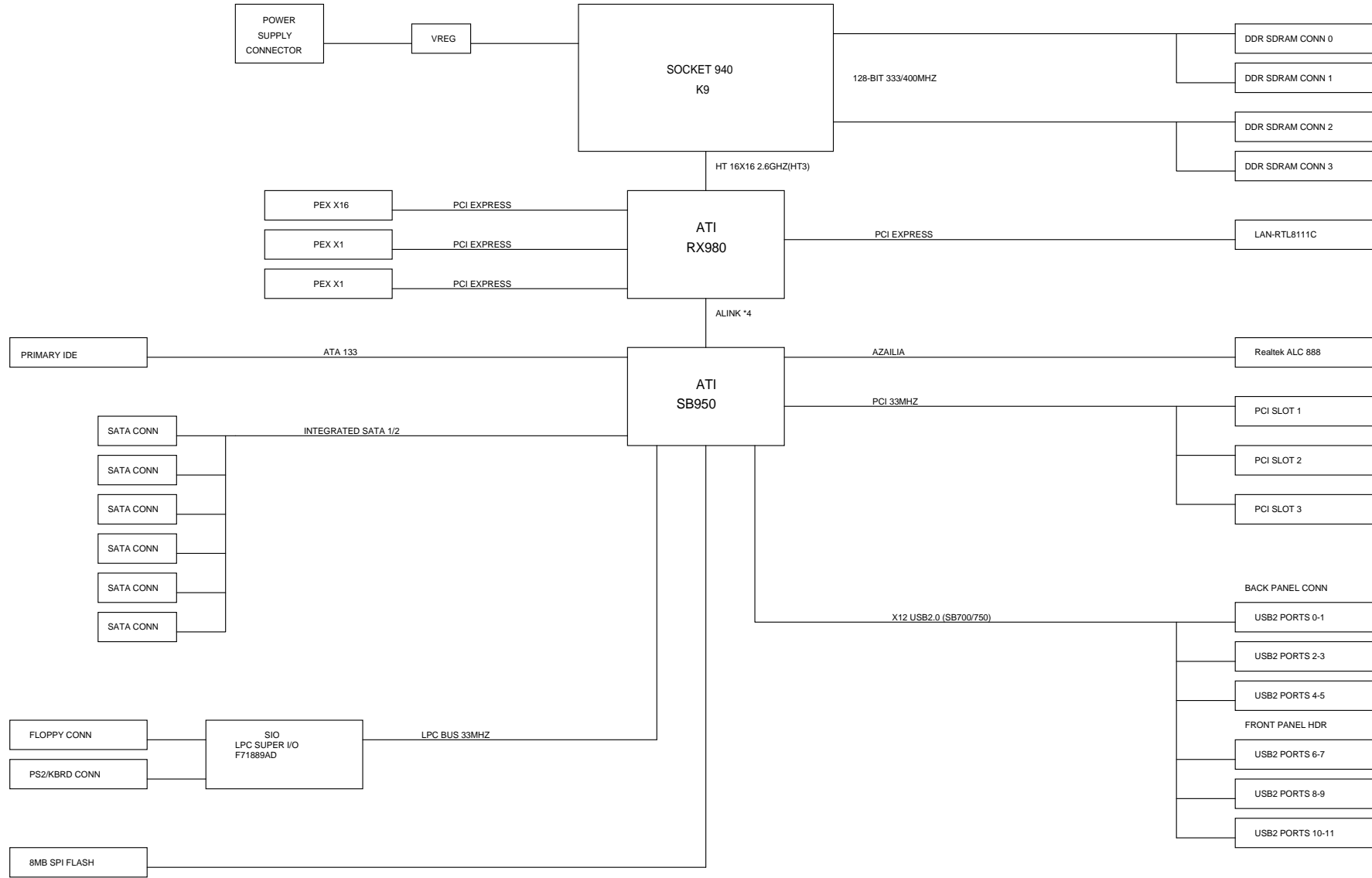
Vnb 1 Phase (MOS HIGHX1 LOWX2)

Clock Generator

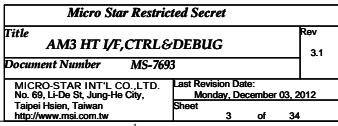
Controller--RTM880N-793

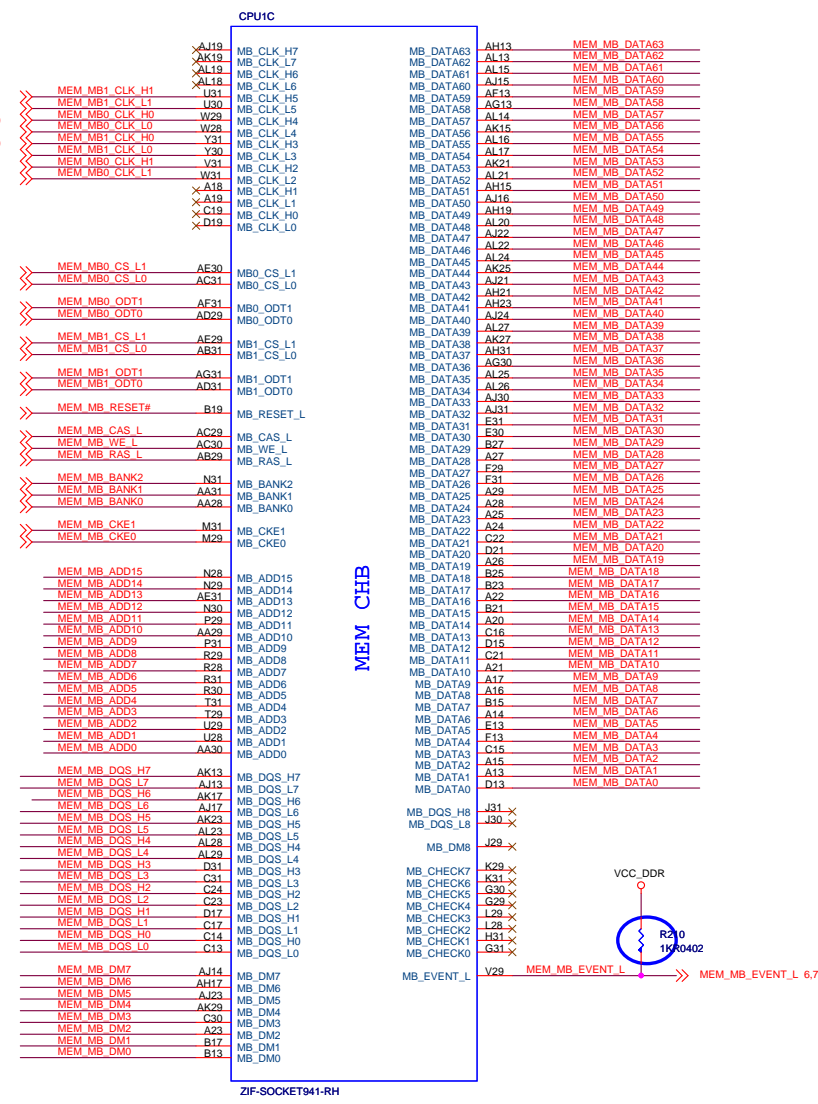
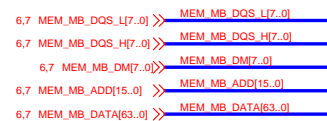
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BLOCK DIAGRAM

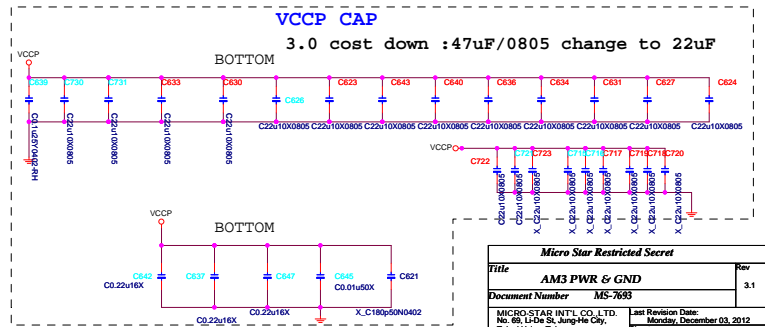
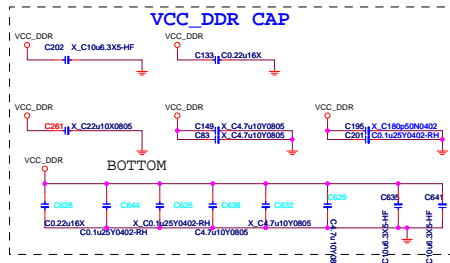
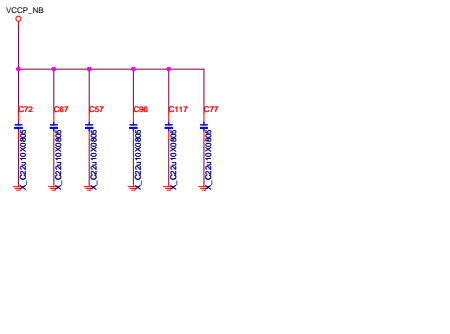
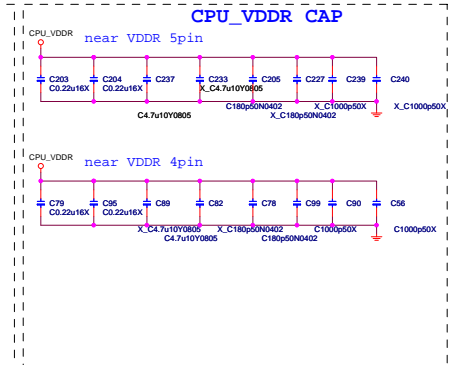
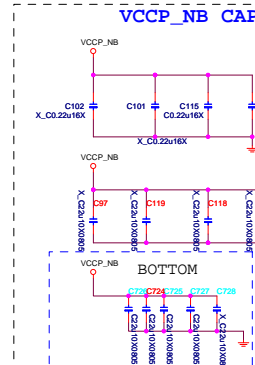
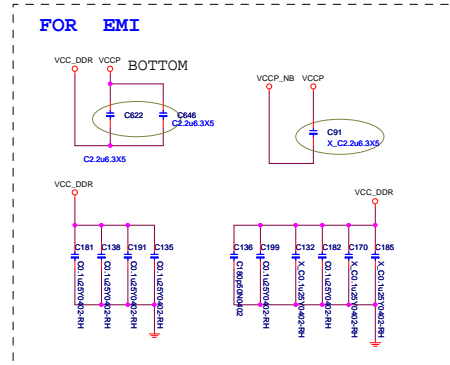
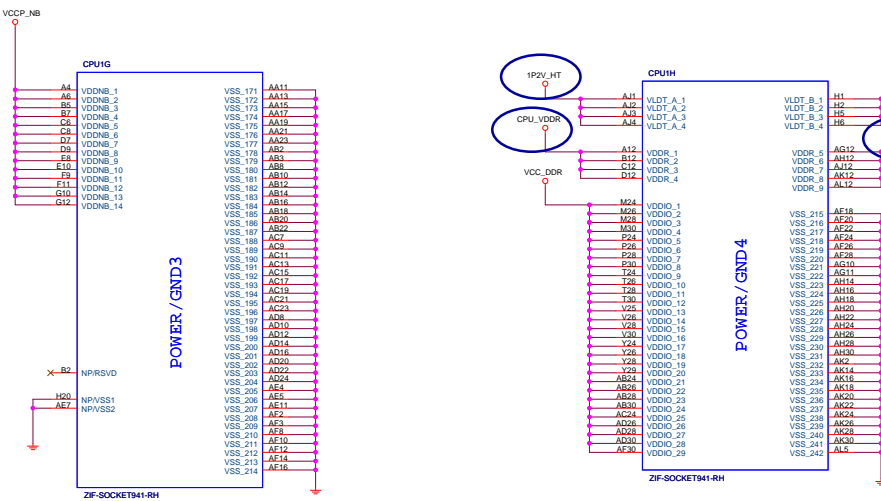
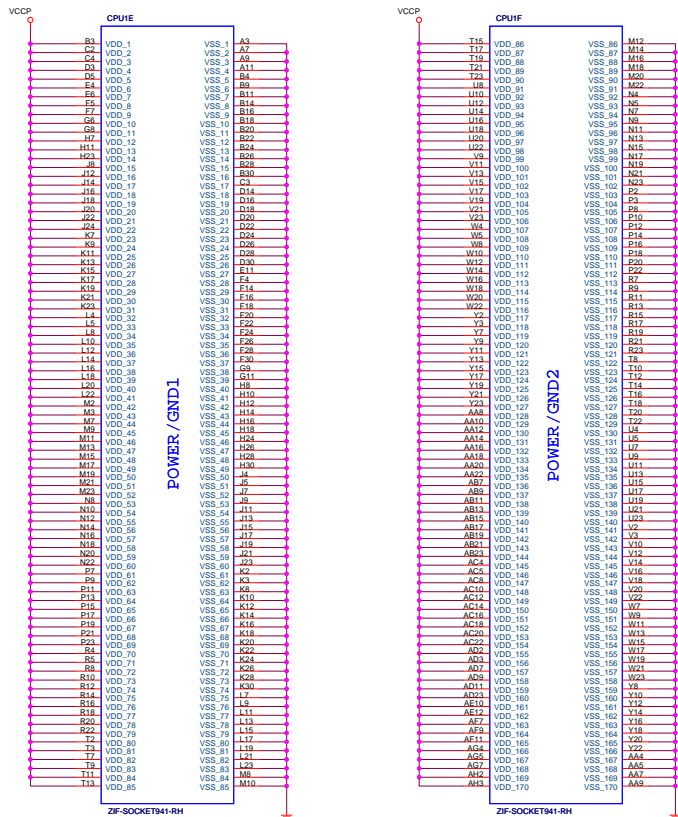


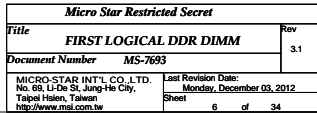
Micro Star Restricted Secret		
Title	Block Diagram	Rev
Document Number	MS-7693	3.0
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St., Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Thursday, October 11, 2012
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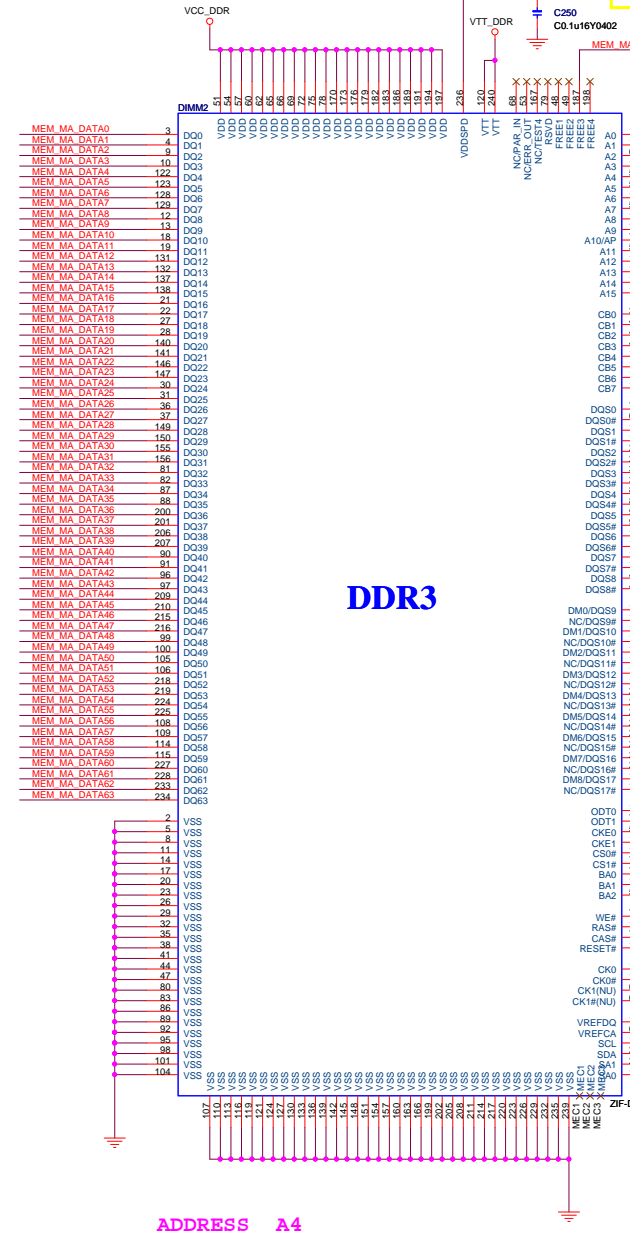


VCCP:110A
VCCNB:20A
1P2V_HT:2.5A
CPU_VDDR:4A
VCC_DDR:5A



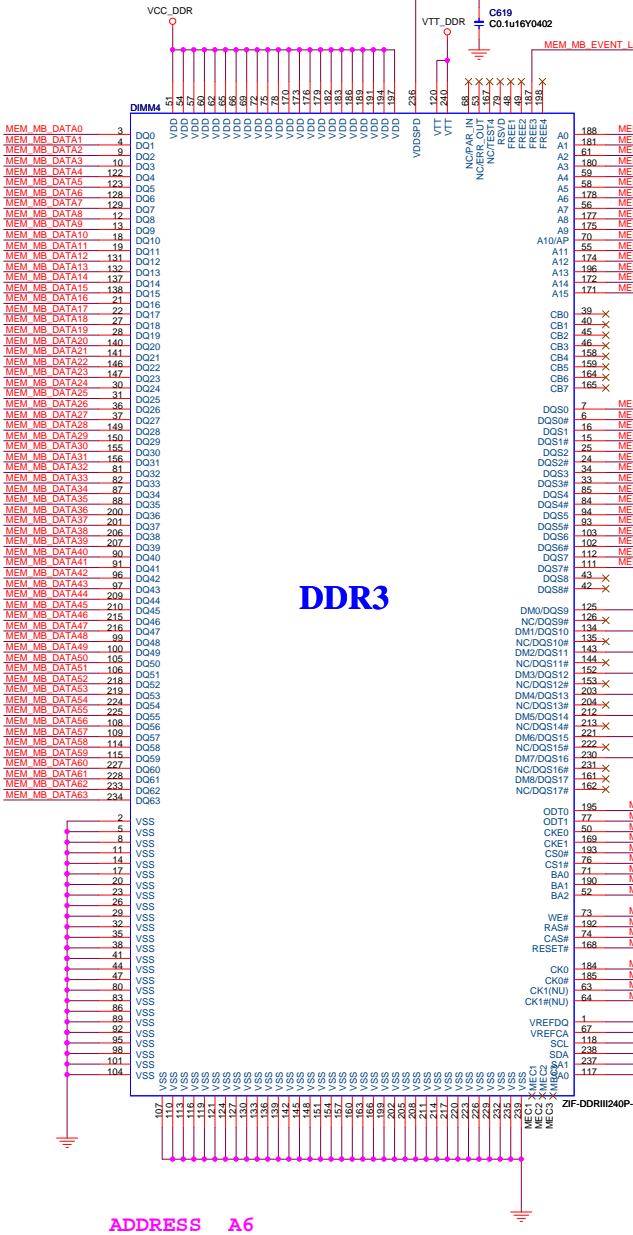


4.6 MEM_MA_DQS_H[7..0] >> MEM_MA_DQS_H[7..0]
4.6 MEM_MA_DQS_L[7..0] >> MEM_MA_DQS_L[7..0]
4.6 MEM_MA_DM[7..0] >> MEM_MA_DM[7..0]
4.6 MEM_MA_ADD[15..0] >> MEM_MA_ADD[15..0]
4.6 MEM_MA_DATA[63..0] >> MEM_MA_DATA[63..0]



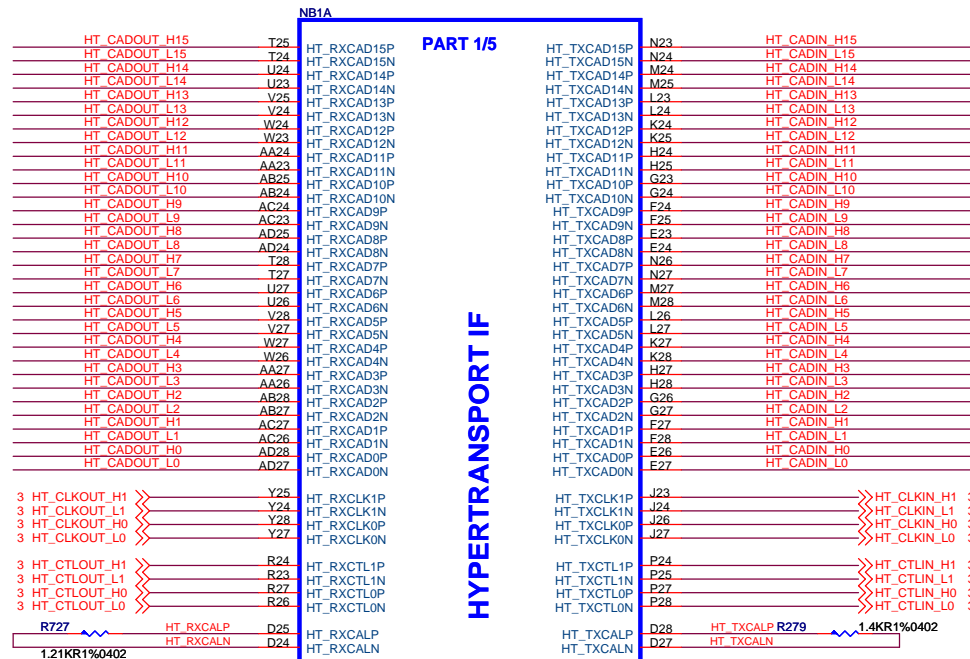
DDR3

4.6 MEM_MB_DQS_L[7..0] >> MEM_MB_DQS_L[7..0]
4.6 MEM_MB_DQS_H[7..0] >> MEM_MB_DQS_H[7..0]
4.6 MEM_MB_DM[7..0] >> MEM_MB_DM[7..0]
4.6 MEM_MB_ADD[15..0] >> MEM_MB_ADD[15..0]
4.6 MEM_MB_DATA[63..0] >> MEM_MB_DATA[63..0]



DDR3

3 HT_CADIN_H[15..0] >> HT_CADIN_H[15..0]
3 HT_CADIN_L[15..0] >> HT_CADIN_L[15..0]
3 HT_CADOUT_H[15..0] >> HT_CADOUT_H[15..0]
3 HT_CADOUT_L[15..0] >> HT_CADOUT_L[15..0]



AMD-215-0716010-00-A21-RH

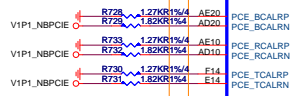
Micro Star Restricted Secret		
Title	RD780-HT LINK I/F	Rev
Document Number	MS-7963	3.1
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St., Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Monday, December 03, 2012
		Sheet 8 of 34

19	GF_X_RX15P	N6	GF_X_RX15P	N3	GF_X_TX15P	19
19	GF_X_RX15N	N5	GF_X_RX15N	A2	GF_X_TX15N	19
19	GF_X_RX14P	M5	GF_X_RX14P	M2	GF_X_TX14P	19
19	GF_X_RX14N	M4	GF_X_RX14N	M1	GF_X_TX14N	19
19	GF_X_RX13P	L6	GF_X_RX13P	L3	GF_X_TX13P	19
19	GF_X_RX13N	L5	GF_X_RX13N	L2	GF_X_TX13N	19
19	GF_X_RX12P	K6	GF_X_RX12P	K2	GF_X_TX12P	19
19	GF_X_RX12N	K4	GF_X_RX12N	K1	GF_X_TX12N	19
19	GF_X_RX11P	J6	GF_X_RX11P	J2	GF_X_TX11P	19
19	GF_X_RX11N	J5	GF_X_RX11N	J1	GF_X_TX11N	19
19	GF_X_RX10P	H6	GF_X_RX10P	H2	GF_X_TX10P	19
19	GF_X_RX10N	H4	GF_X_RX10N	H1	GF_X_TX10N	19
19	GF_X_RX9P	G6	GF_X_RX9P	G3	GF_X_TX9P	19
19	GF_X_RX9N	G5	GF_X_RX9N	G2	GF_X_TX9N	19
19	GF_X_RX8P	F6	GF_X_RX8P	F2	GF_X_TX8P	19
19	GF_X_RX8N	F4	GF_X_RX8N	F1	GF_X_TX8N	19
19	GF_X_RX7P	D6	GF_X_RX7P	D2	GF_X_TX7P	19
19	GF_X_RX7N	D1	GF_X_RX7N	D1	GF_X_TX7N	19
19	GF_X_RX6P	C6	GF_X_RX6P	C4	GF_X_TX6P	19
19	GF_X_RX6N	C5	GF_X_RX6N	C4	GF_X_TX6N	19
19	GF_X_RX5P	D6	GF_X_RX5P	A6	GF_X_TX5P	19
19	GF_X_RX5N	E6	GF_X_RX5N	B6	GF_X_TX5N	19
19	GF_X_RX4P	E7	GF_X_RX4P	B7	GF_X_TX4P	19
19	GF_X_RX4N	F7	GF_X_RX4N	C7	GF_X_TX4N	19
19	GF_X_RX3P	D6	GF_X_RX3P	A6	GF_X_TX3P	19
19	GF_X_RX3N	E8	GF_X_RX3N	B8	GF_X_TX3N	19
19	GF_X_RX2P	F9	GF_X_RX2P	C9	GF_X_TX2P	19
19	GF_X_RX2N	F9	GF_X_RX2N	C9	GF_X_TX2N	19
19	GF_X_RX1P	D10	GF_X_RX1P	A10	GF_X_TX1P	19
19	GF_X_RX1N	E10	GF_X_RX1N	B10	GF_X_TX1N	19
19	GF_X_RX0P	F11	GF_X_RX0P	B11	GF_X_TX0P	19
19	GF_X_RX0N	F11	GF_X_RX0N	C11	GF_X_TX0N	19

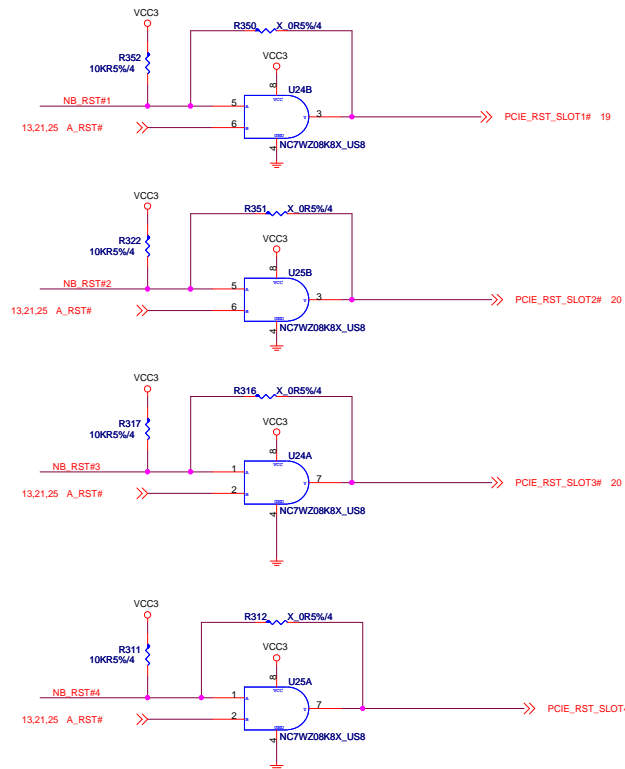
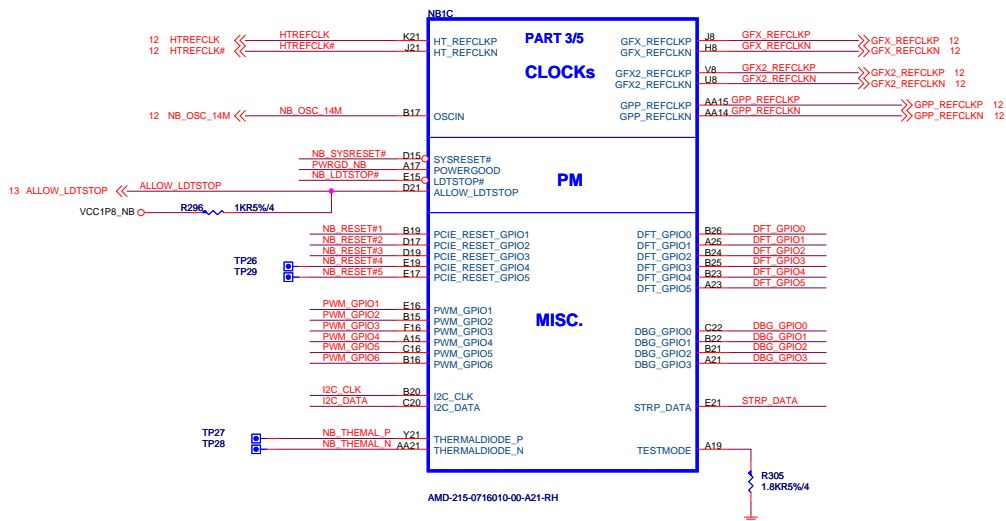
AC9	GF_X_RX15P	GF_X_TX15P	AE9
AD9	GF_X_RX15N	GF_X_TX15N	AE9
AD8	GF_X_RX14P	GF_X_TX14P	AE8
AE8	GF_X_RX14N	GF_X_TX14N	AE8
AD7	GF_X_RX13P	GF_X_TX13P	AE7
AD7	GF_X_RX13N	GF_X_TX13N	AE7
AE6	GF_X_RX12P	GF_X_TX12P	AE6
AE6	GF_X_RX12N	GF_X_TX12N	AE6
AE5	GF_X_RX11P	GF_X_TX11P	AE5
AE5	GF_X_RX11N	GF_X_TX11N	AE5
AE4	GF_X_RX10P	GF_X_TX10P	AE4
AD2	GF_X_RX9P	GF_X_TX9P	AE3
AD1	GF_X_RX9N	GF_X_TX9N	AE3
AB5	GF_X_RX8P	GF_X_TX8P	AE2
AB4	GF_X_RX8N	GF_X_TX8N	AE2
AA6	GF_X_RX7P	GF_X_TX7P	AE1
AA5	GF_X_RX7N	GF_X_TX7N	AE1
Y4	GF_X_RX6P	GF_X_TX6P	Y2
Y4	GF_X_RX6N	GF_X_TX6N	Y2
W6	GF_X_RX5P	GF_X_TX5P	W3
W5	GF_X_RX5N	GF_X_TX5N	W2
V5	GF_X_RX4P	GF_X_TX4P	V2
V4	GF_X_RX4N	GF_X_TX4N	V1
U6	GF_X_RX3P	GF_X_TX3P	U2
U5	GF_X_RX3N	GF_X_TX3N	U1
T4	GF_X_RX2P	GF_X_TX2P	T2
T4	GF_X_RX2N	GF_X_TX2N	T1
R6	GF_X_RX1P	GF_X_TX1P	R2
R5	GF_X_RX1N	GF_X_TX1N	R1
P5	GF_X_RX0P	GF_X_TX0P	P2
P4	GF_X_RX0N	GF_X_TX0N	P1

AD11	GPP_RX9P	GPP_TX9P	AH19
AD11	GPP_RX9N	GPP_TX9N	AH19
AE12	GPP_RX8P	GPP_TX8P	AG19
AD12	GPP_RX8N	GPP_TX8N	AG19
AD13	GPP_RX7P	GPP_TX7P	AG18
AD13	GPP_RX7N	GPP_TX7N	AG18
AE14	GPP_RX6P	GPP_TX6P	AG18
AD14	GPP_RX6N	GPP_TX6N	AG18
AD15	GPP_RX5P	GPP_TX5P	AH17
AE15	GPP_RX5N	GPP_TX5N	AG17
AE16	GPP_RX4P	GPP_TX4P	AG17
AD16	GPP_RX4N	GPP_TX4N	AG17
AD17	GPP_RX3P	GPP_TX3P	AH16
AE17	GPP_RX3N	GPP_TX3N	AG16
AD18	GPP_RX2P	GPP_TX2P	AG17
AD18	GPP_RX2N	GPP_TX2N	AG17
AD19	GPP_RX1P	GPP_TX1P	AH18
AE19	GPP_RX1N	GPP_TX1N	AG18
AH20	GPP_RX0P	GPP_TX0P	AG19
AG20	GPP_RX0N	GPP_TX0N	AE19

13	A_RX3P	A_RX3P	AC21	SB_RX3P	AG22	A_TX3P	C659	C01u10X0402	A_TX3P	13
13	A_RX3N	A_RX3P	AD21	SB_RX3N	AH22	A_TX3N	C658	C01u10X0402	A_TX3N	13
13	A_RX2P	A_RX2P	AD22	SB_RX2P	AG21	A_TX2P	C655	C01u10X0402	A_TX2P	13
13	A_RX2N	A_RX2N	AE22	SB_RX2N	AG21	A_TX2N	C657	C01u10X0402	A_TX2N	13
13	A_RX1P	A_RX1P	AG25	SB_RX1P	AG23	A_TX1P	C654	C01u10X0402	A_TX1P	13
13	A_RX1N	A_RX1N	AG25	SB_RX1N	AG23	A_TX1N	C652	C01u10X0402	A_TX1N	13
13	A_RX0P	A_RX0P	AG26	SB_RX0P	AG24	A_TX0P	C651	C01u10X0402	A_TX0P	13
13	A_RX0N	A_RX0N	AG26	SB_RX0N	AG24	A_TX0N	C649	C01u10X0402	A_TX0N	13



Spacing : 6mil
AMD-215-0716010-00-A21-RH



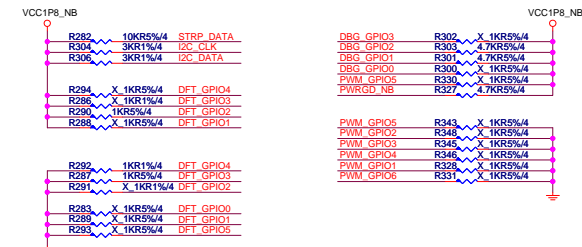
PWM_GPIO[5:2]

Reserved.

Make provision for an external pull-down resistor on each of the pins, but do not install a resistor.

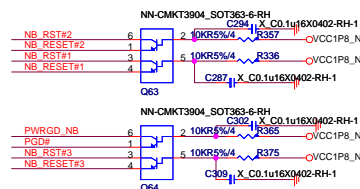
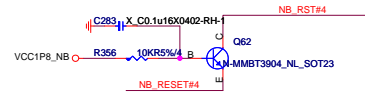
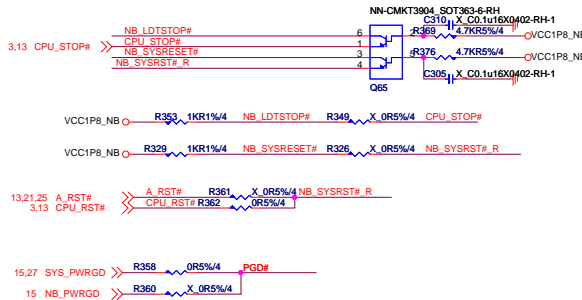
DFT_GPIO0

Reserved. Make provision for an external pull-down resistor on this pin, but do not install a resistor.



DFT_GPIO[4:2]
STRAP_PCIE_GPP_CFG

111: 1-1-1-1-1-1	Mode L
110: 1-1-1-1-1-1	Mode L
101: 2-0-2-0-2-0	Mode C2
100: 2-0-2-0-1-1	Mode K
011: 2-0-1-1-1-1	Mode E
010: 1-1-1-1-1-1	Mode L
001: 4-0-0-0-1-1	Mode C default
000: 4-0-0-0-2-0	Mode B



DFT_GPIO1

Selects loading of strap values from EEPROM

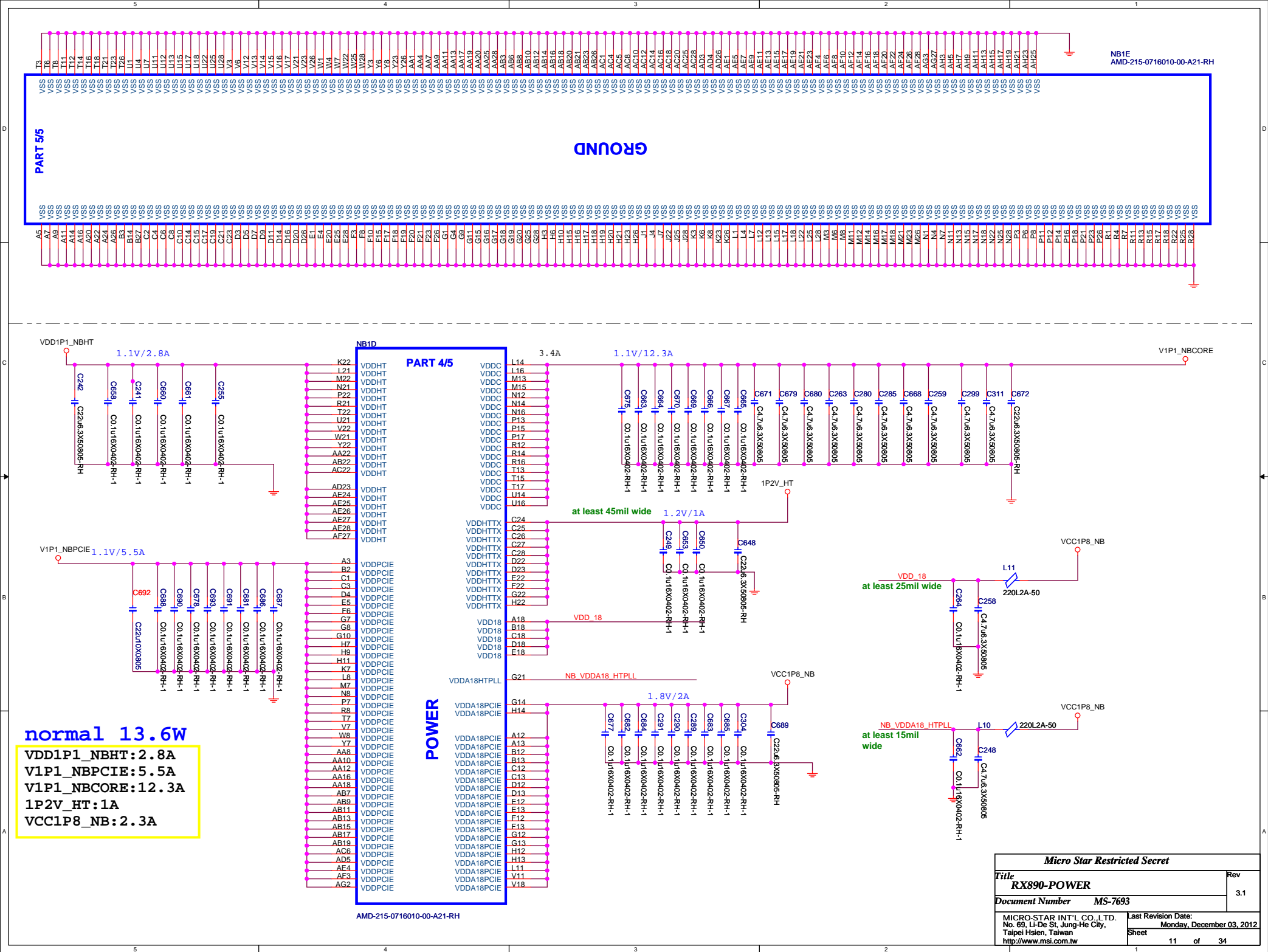
0: I2C master can load strap values from EEPROM if connected, or use hardware default values if not connected

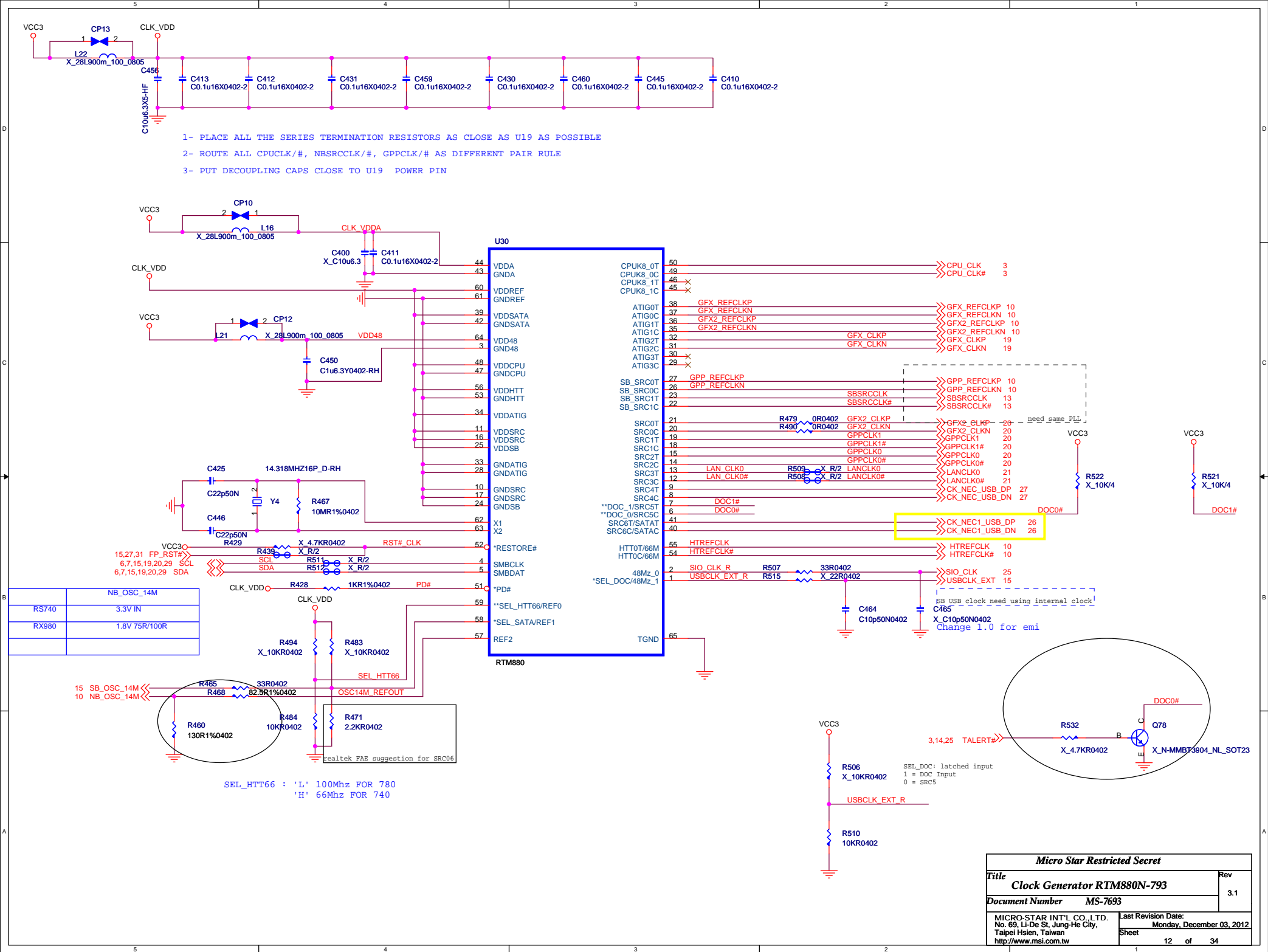
1: Use hardware default values (Default)

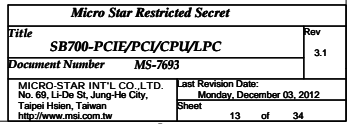
DFT_GPIO5

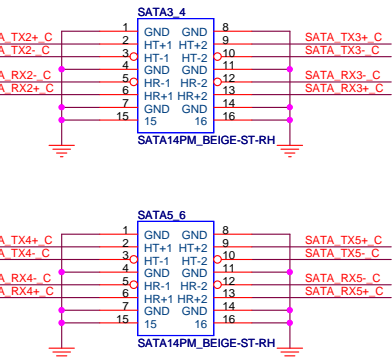
Reserved. Make provision for an external pull-down resistor on this pin, but do not install a resistor.

Micro Star Restricted Secret		
Title	RD780-SYSTEM I/F	Rev
Document Number	MS-7693	3.1
MICRO-STAR INT'L CO., LTD. No. 68, Li-De St., Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		
Last Revision Date:		Monday, December 03, 2012
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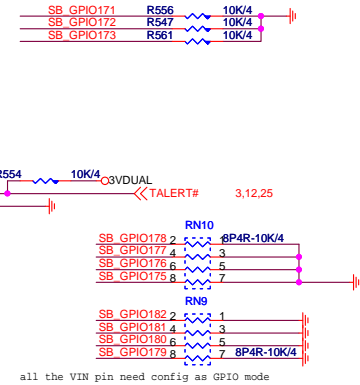
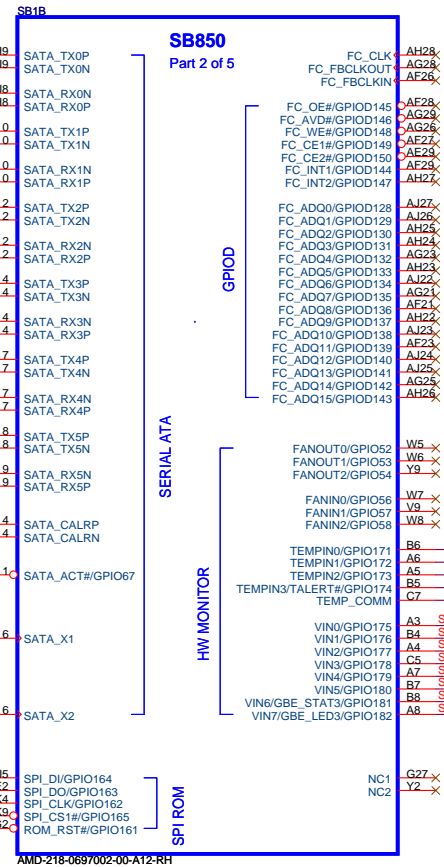
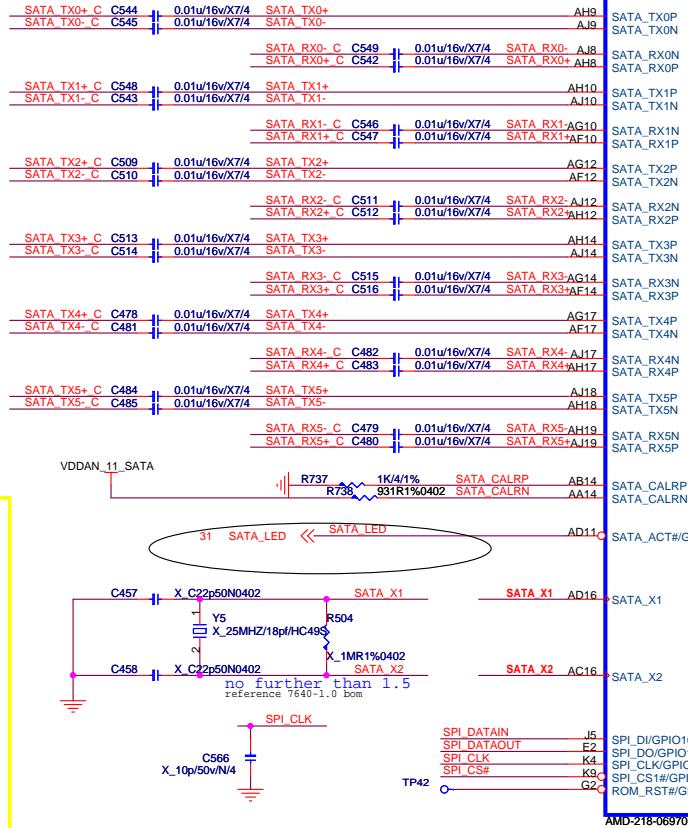




3.0 change to connector with 90 degree

Gen3: Signal length from the Southbridge to connector = 2.5".

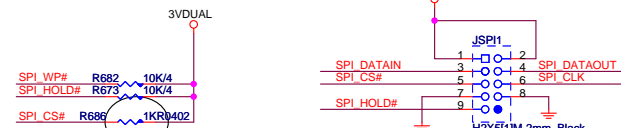
SATA_TX[5:0]P/N: Routed with 90-ohm $\text{\textcircled{R}}$ 10% differential impedance.
SATA_RX[5:0]P/N: Routed with 90-ohm $\text{\textcircled{R}}$ 10% differential impedance.



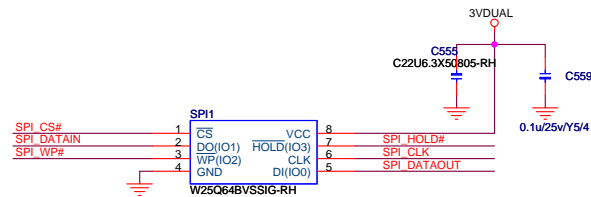
all the VIN pin need config as GPIO mode

SPI FLASH MEMORY

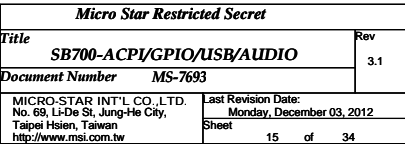
SPI DEBUG PORT
Place close to SPI ROM

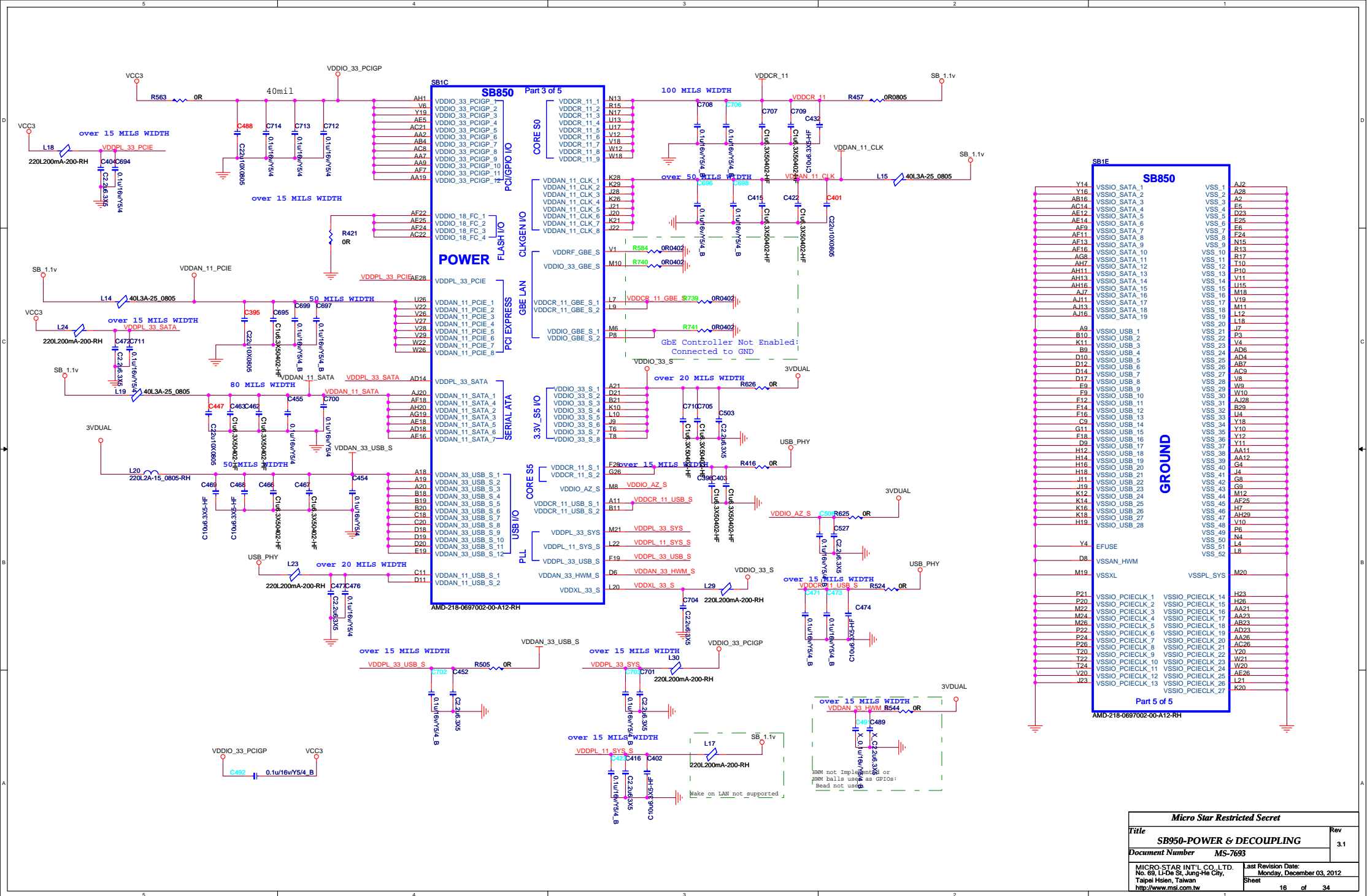


Part Number : N31-2051451-H06



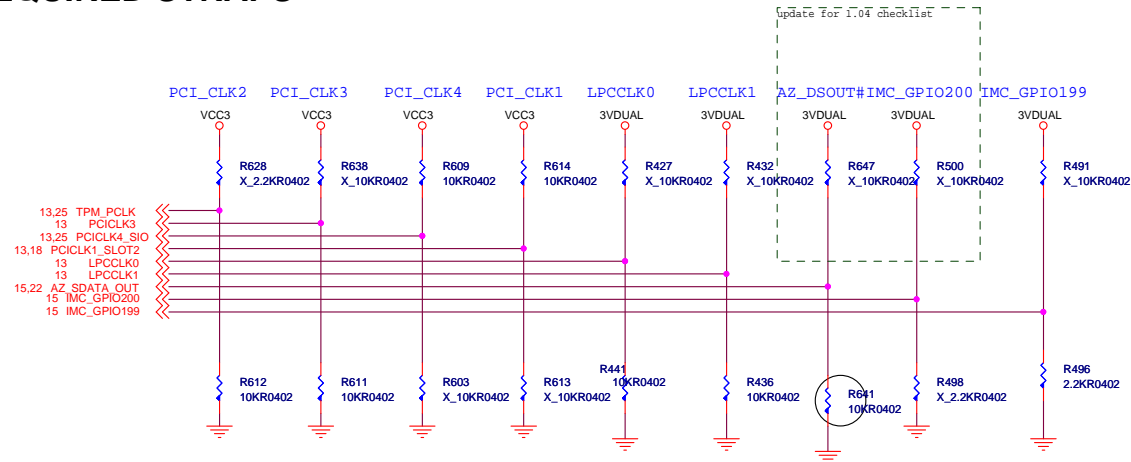
Micro Star Restricted Secret		
Title	Rev	
SB700-SATA/IDE/HWM/SPI		
Document Number	MS-7693	3.1
MICRO-STAR INT'L CO., LTD. No. 68, Li-Ho St., Jung-Ho City, Taipei Hsien, Taiwan		Last Revision Date: Monday, December 03, 2012
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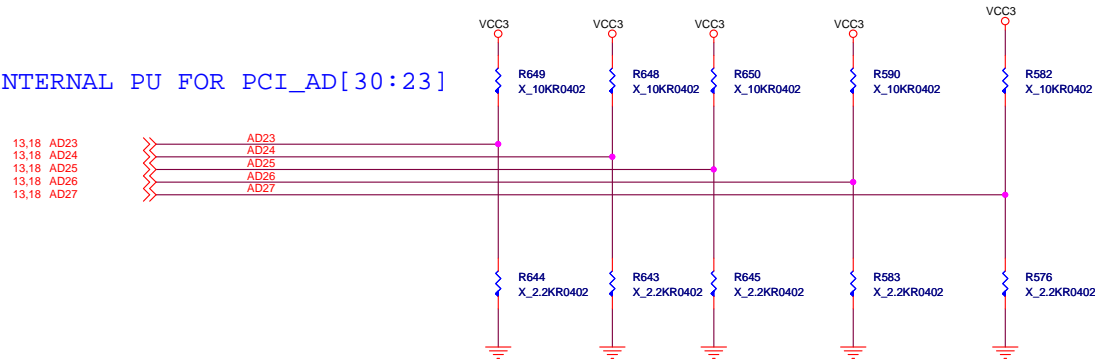
REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_DOUT#	IMC_GPIO200	IMC_GPIO199
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	NON-FUSION CPU CLOCK MODE DEFAULT	UEC ENABLE	CLKGEN ENABLED		ROM TYPE: H, H = Reserved H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	DEFAULT
PULL LOW	FORCE PCIE GEN1	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	FUSION CPU CLOCK MODE	DISABLE EC DEFAULT	CLKGEN DISABLED DEFAULT	PERFORMANCE MODE DEFAULT		

SB800 HAS 15K INTERNAL PU FOR PCI_AD[30:23]



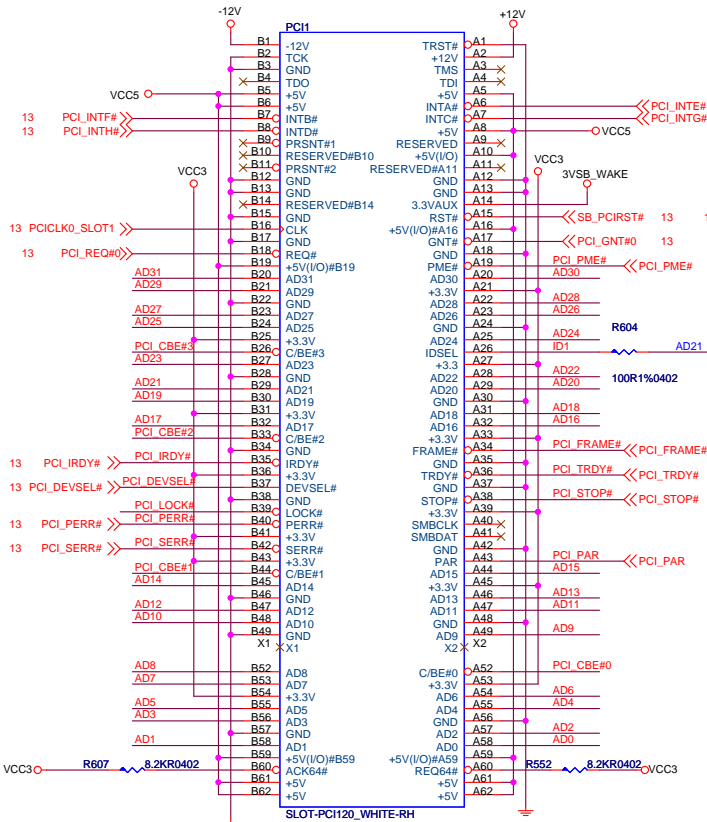
DEBUG STRAPS

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Micro Star Restricted Secret	
Title SB950-STRAPS	Rev 3.1
Document Number MS-7693	Last Revision Date: Monday, December 03, 2012
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw	Sheet 17 of 34

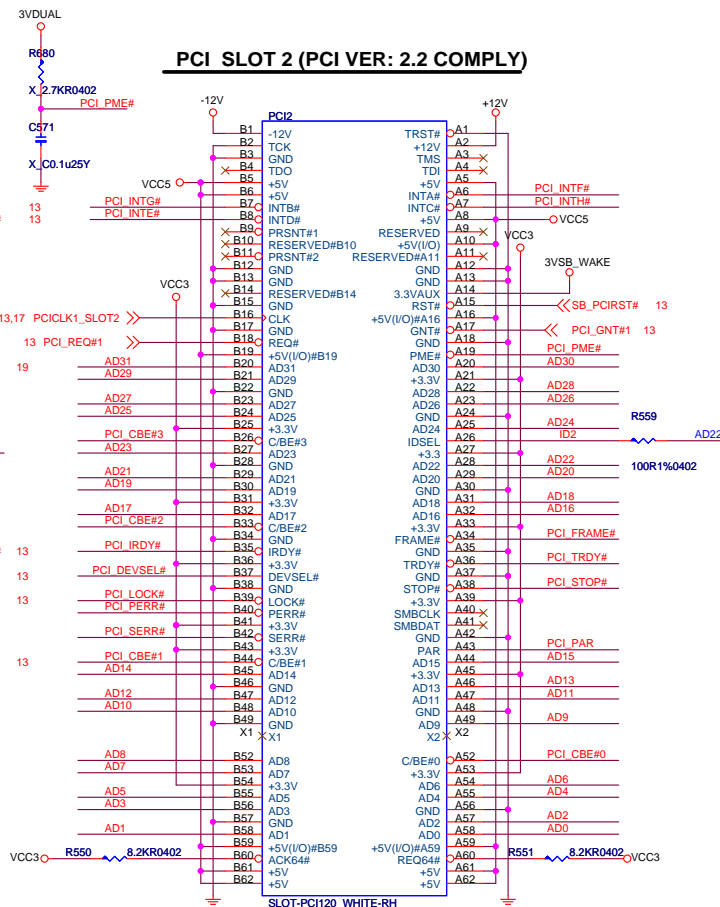
13,17 AD[31..0] >> AD[31..0]
13 PCI_CBE#[3..0] >> PCI_CBE#[3..0]

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



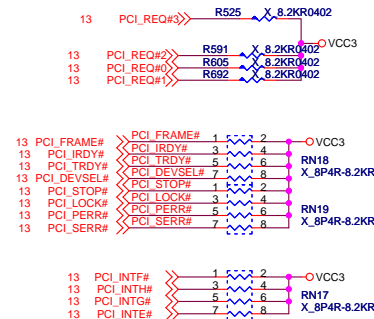
IDSEL = AD21
MASTER = PCI_REQ#0
PCI_GNT#0

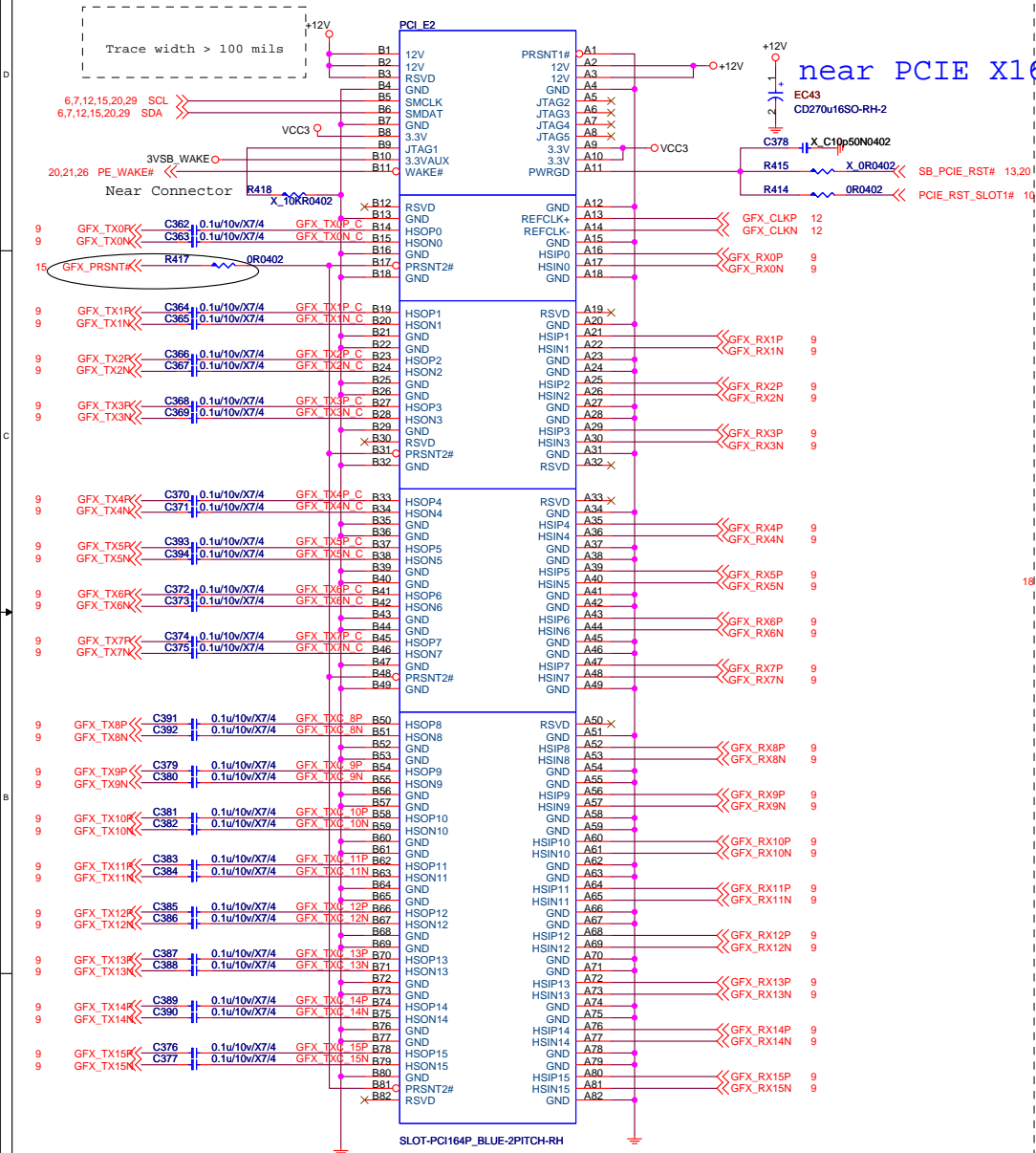
PCI SLOT 2 (PCI VER: 2.2 COMPLY)



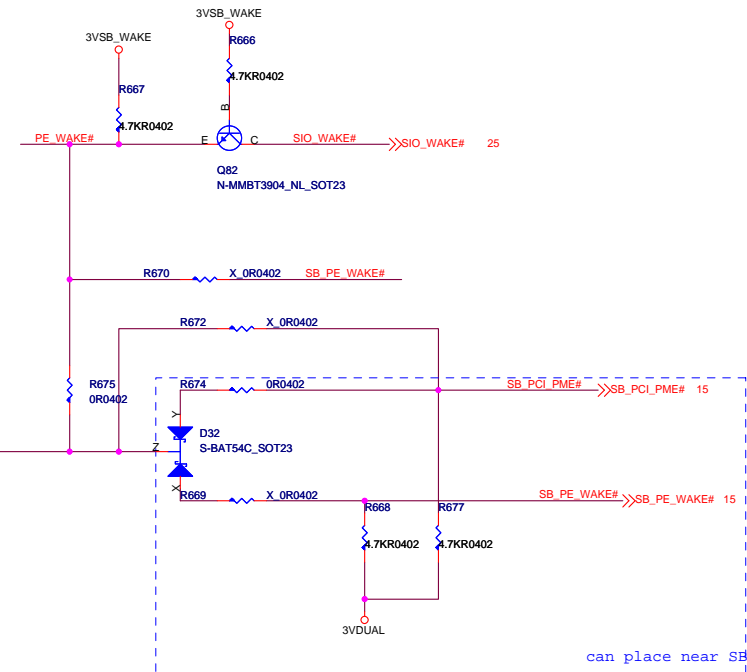
IDSEL = AD22
MASTER = PCI_REQ#1
PCI_GNT#1

PCI PULL-UP / DOWN RESISTORS



PCI EXPRESS_16

near PCIE X16 Slot



can place near SB

Digital Switch SEL pin	SLI function
0	SLI Disabled
1	SLI Enabled

SEL (X8_X8#)	Output	X8_SW	PCI-E_Slot 1/2
Low	Oa	Low	X8 / X8
Hi	Ob	Hi	X16 / 0

Micro Star Restricted Secret

Title	<i>PCI-E X16 , X1 Slot</i>
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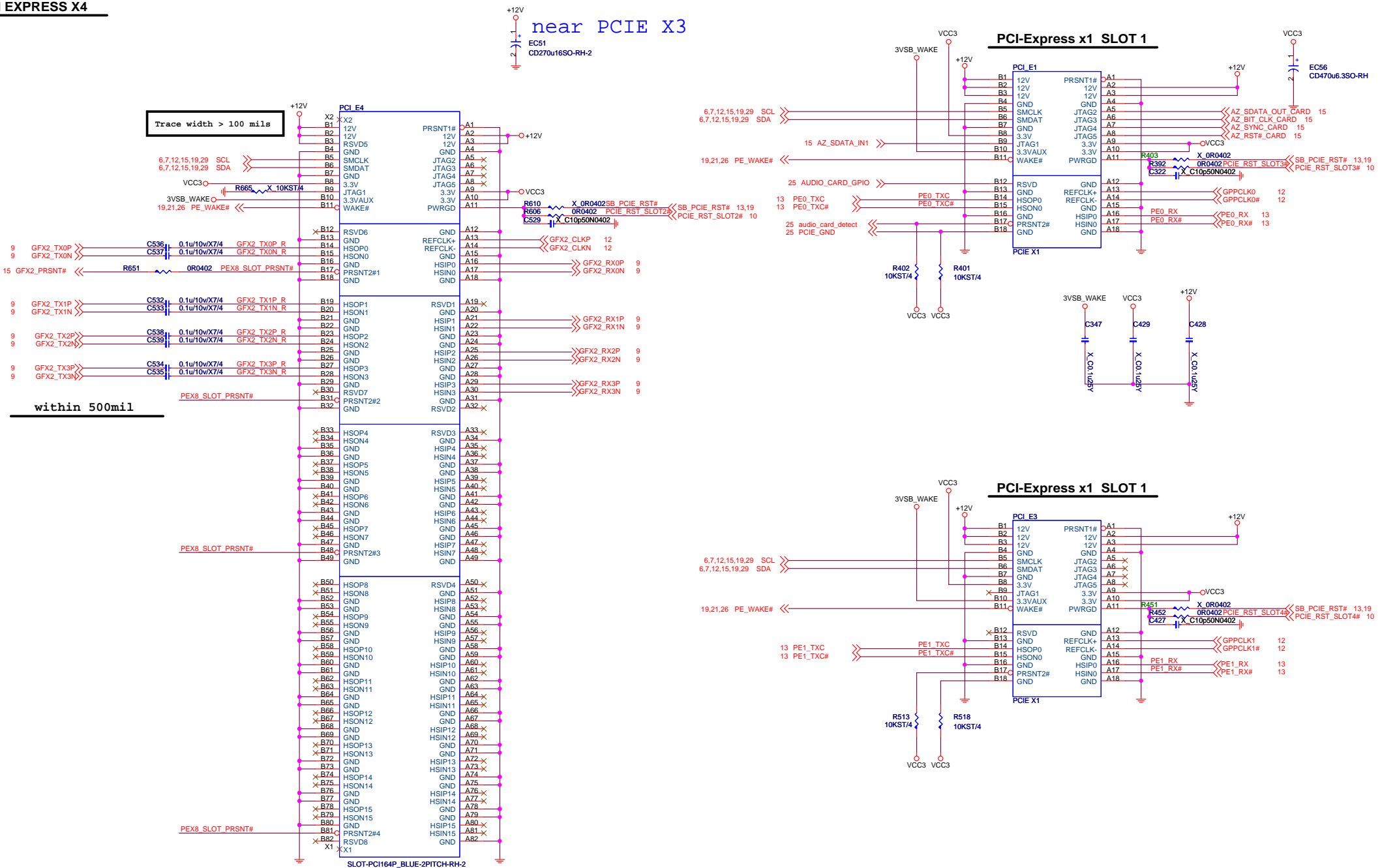
Rev

3.1

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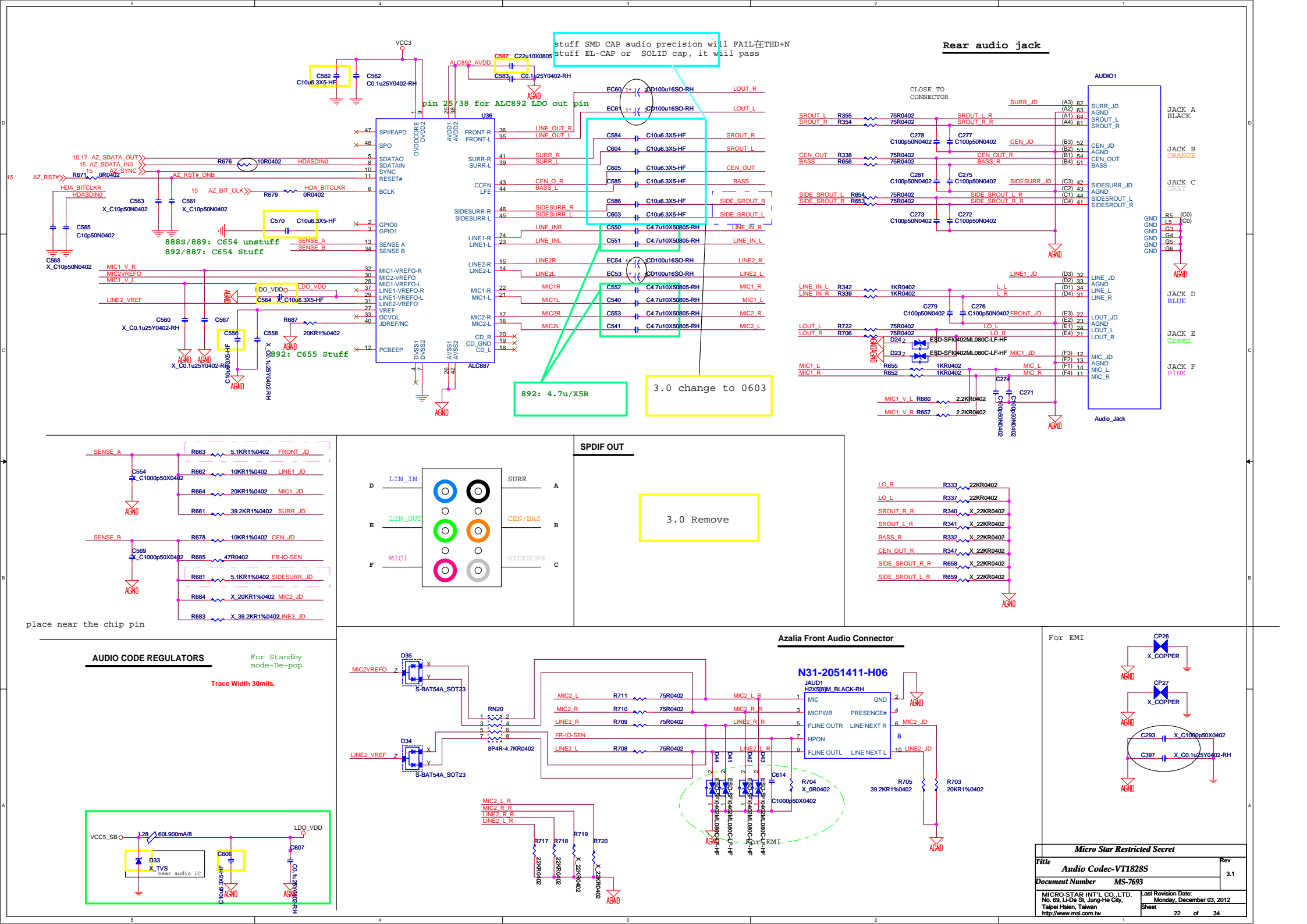
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PCI EXPRESS X4



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Title <i>PCIE X1 Slot 1, 2</i>		Rev 3.1
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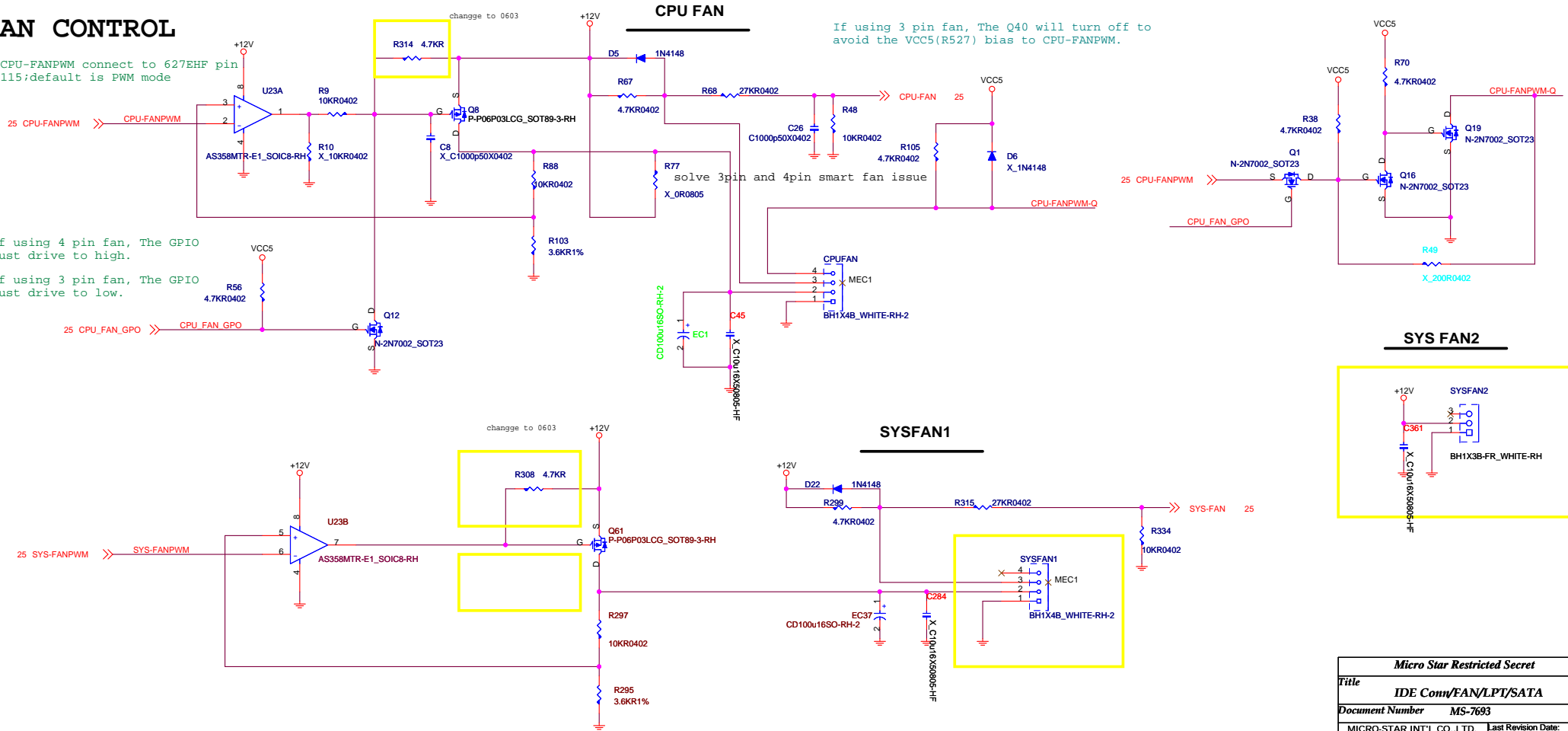
3.0 Remove APS LED

FAN CONTROL

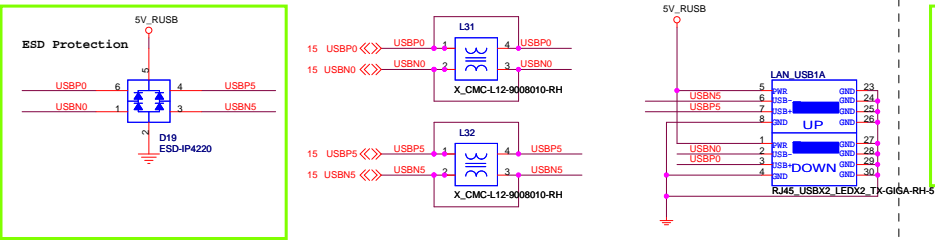
CPU-FANPWM connect to 627EHF pin 115; default is PWM mode

If using 4 pin fan, The GPIO must drive to high.

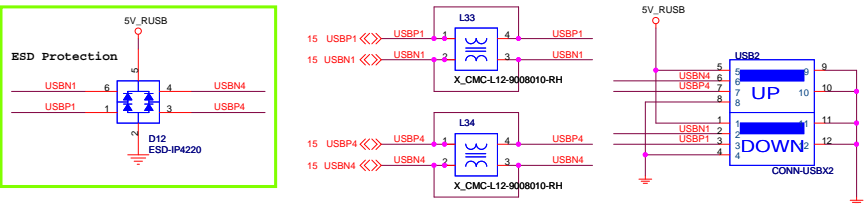
If using 3 pin fan, The GPIO must drive to low.



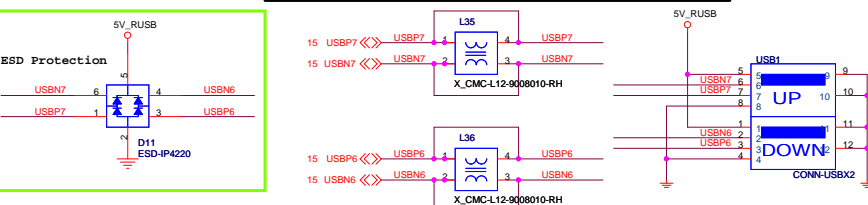
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



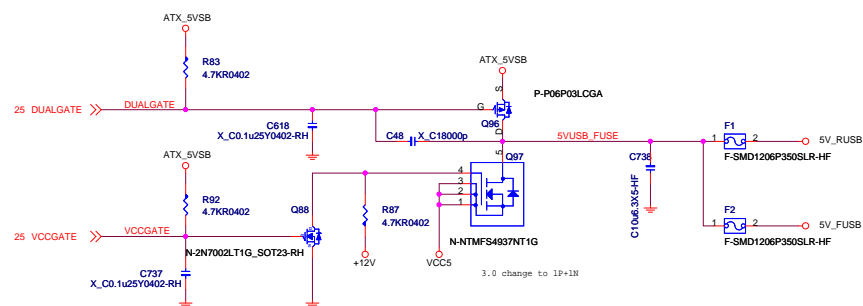
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



REAR PANEL USB CONNECTOR FOR USB PORT 4,5



Type B: MOS+Fuse



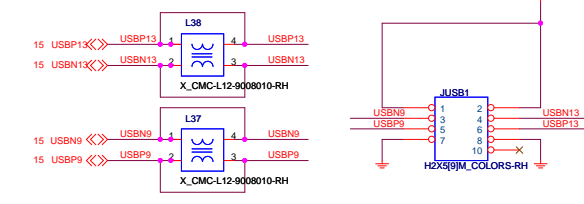
USB2.0 POWER Control			
MODE	S5	S0	S3
DUALGATE	0/1	1	0
VCCGATE	1	0	1

*In S5# DUALGATE pin status is Tri-state, and can be programmed Low level.

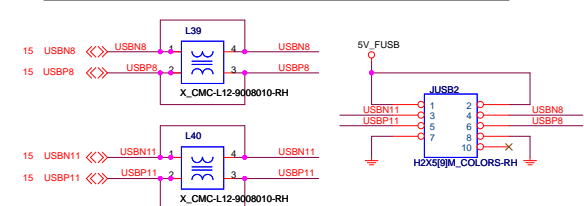
*DUALGATE and VCCGATE can't setting to low together, avoid leakage voltage issue

FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

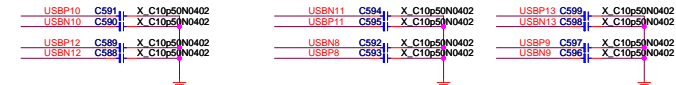
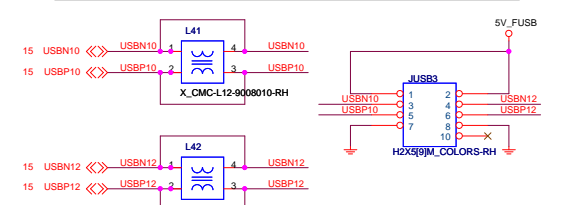
Reversed, can be taken off riser card within bead



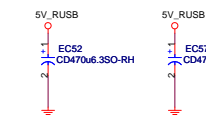
FRONT PANEL USB CONNECTOR FOR USB PORT 8,9



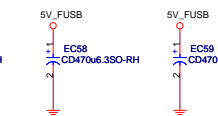
FRONT PANEL USB CONNECTOR FOR USB PORT 10,11



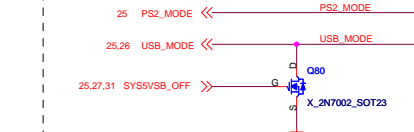
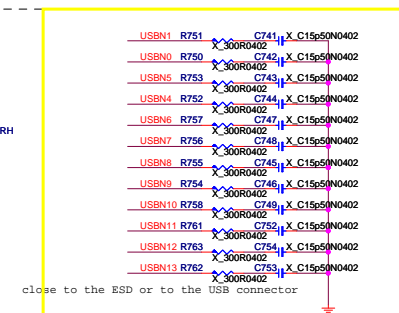
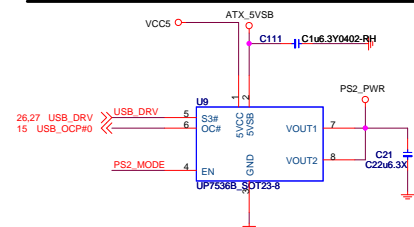
NEAR USB REAR CONNECTOR



NEAR USB Front CONNECTOR



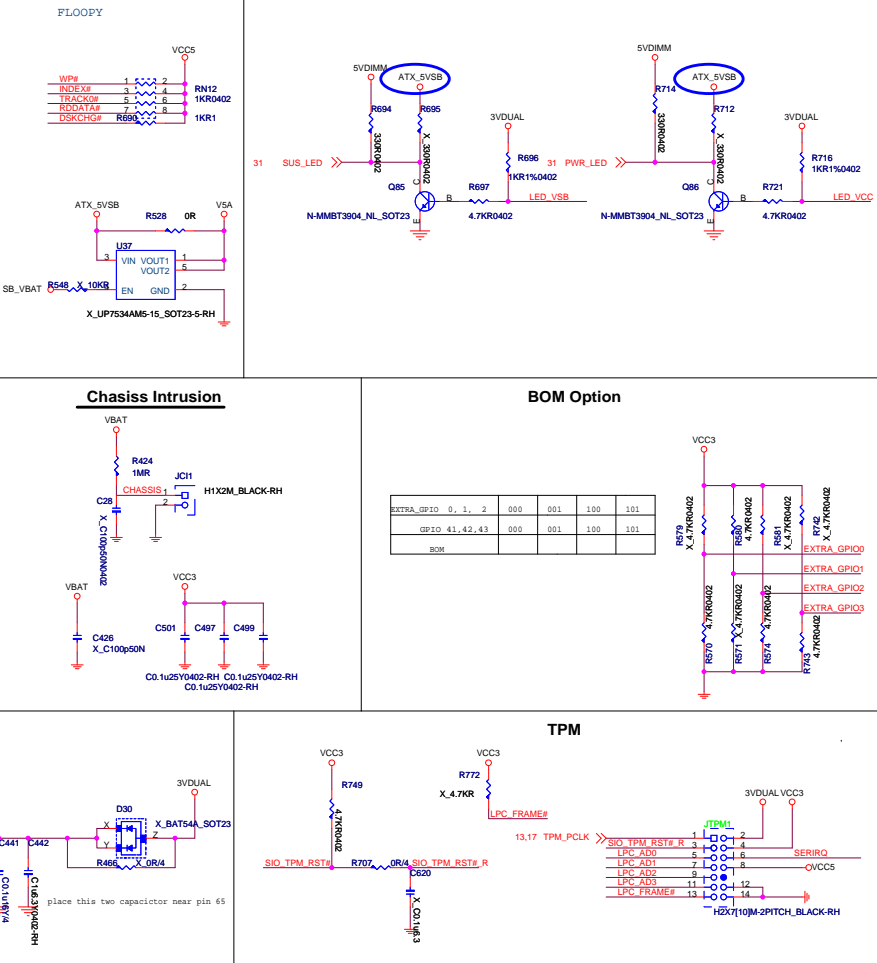
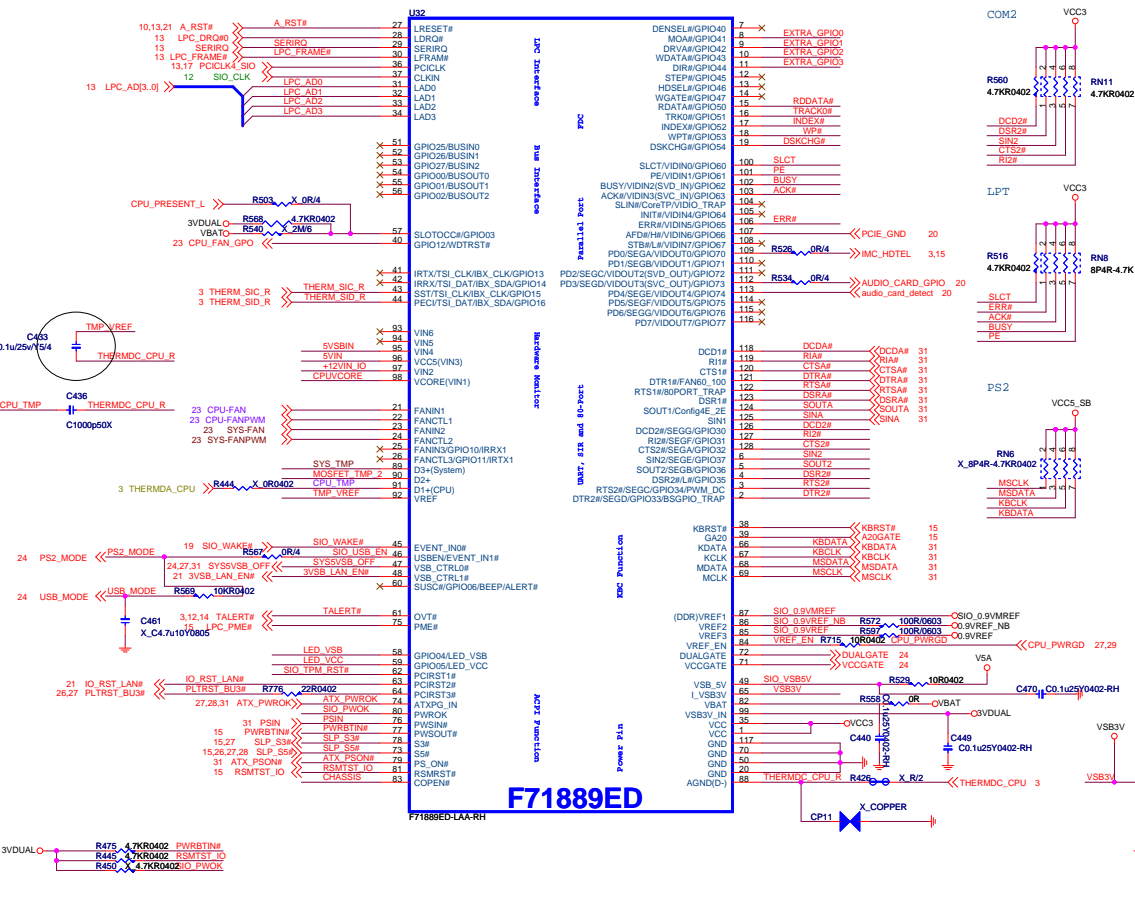
POWER CIRCUIT FOR PS2



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USB CONNECTORS			Rev
Document Number	MS-7693		3.1
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Super I/O

LPC SUPER I/O F71889ED

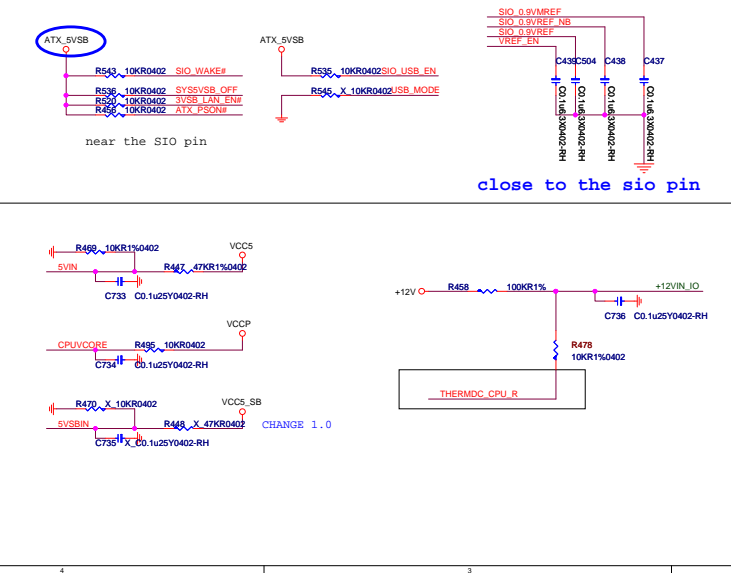


LPC I/O STRAPPING RESISTOR

	Don't STUFF	STUFF
RTS2#	PRM FAN	LINEAR FAN
RTSA#	80Port enable	80Port disable
SOUTA#	4E	2E
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%
SOUT2	OVP warning mode	OVP force mode

near the SIO pin

close to the sio pin



Thermal Resistor

NOTE: LOCATE CLOSE S VRM mosfet for VRM mosfet temperature detect only

Micro Star Restricted Secret

Title: LPC SUPER I/O & LPC & CONNECTORS

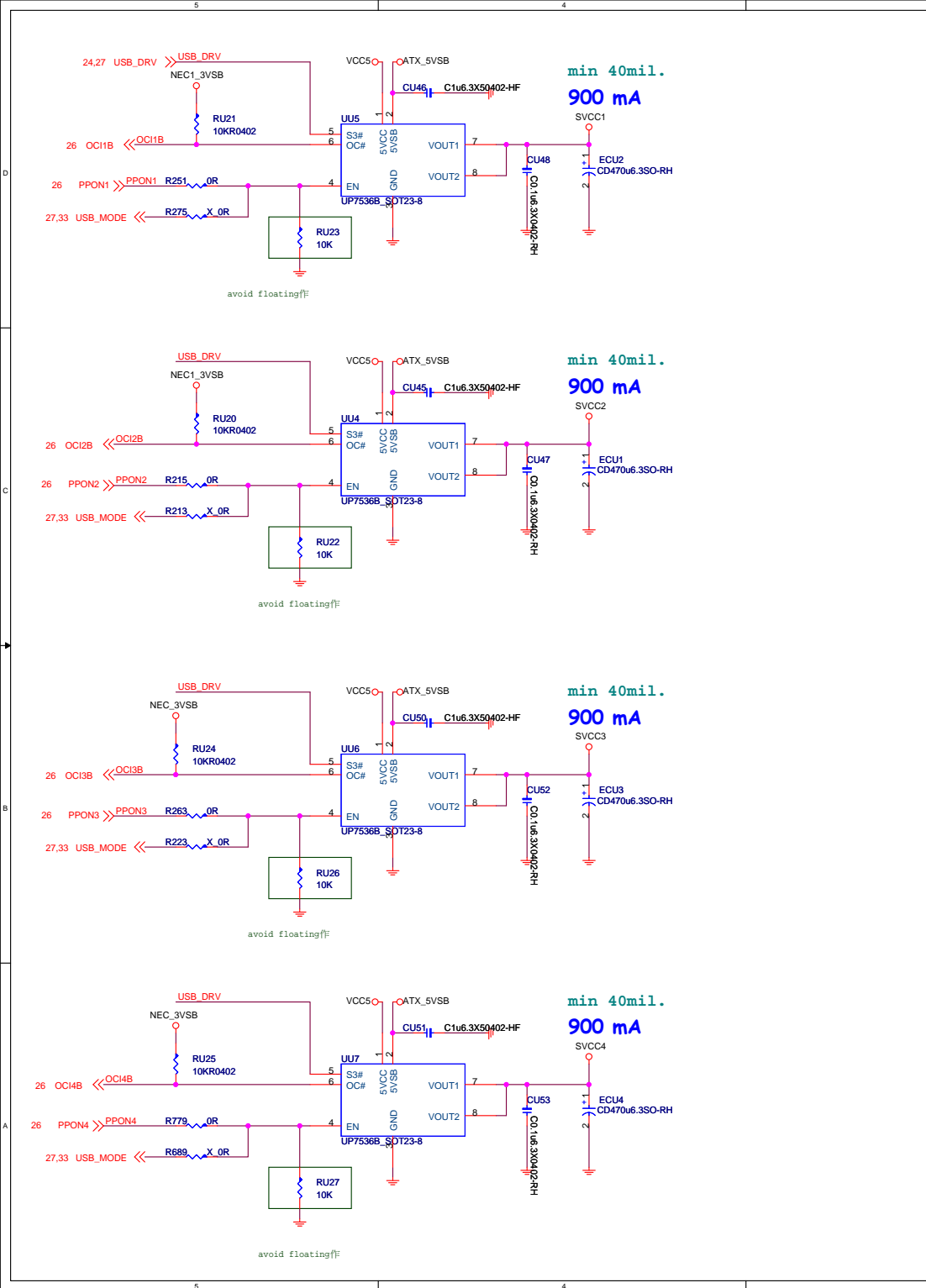
Document Number: MS-7693

Rev: 3.1

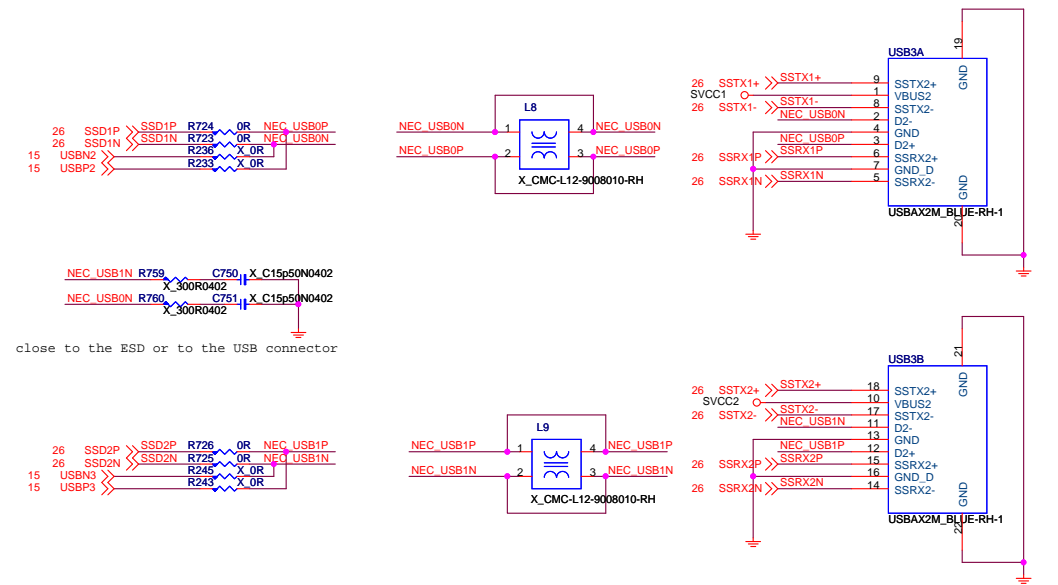
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No. 89, Li-De St., Jung-Ho City,
Taippei Hsien, Taiwan
http://www.msi.com.tw

Last Revision Date:
Monday, December 03, 2012

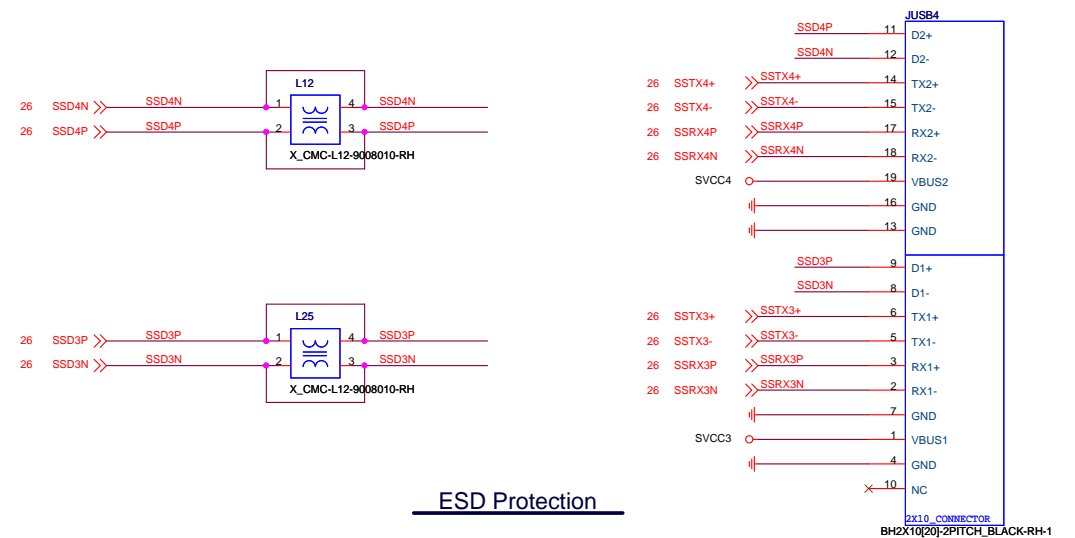
Sheet 25 of 34



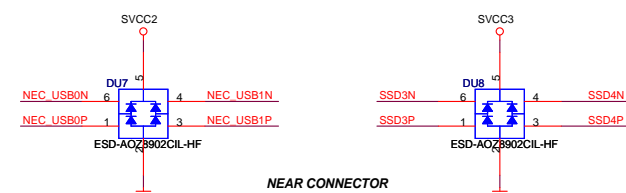
Rear USB3 CONN



Front USB3 CONN

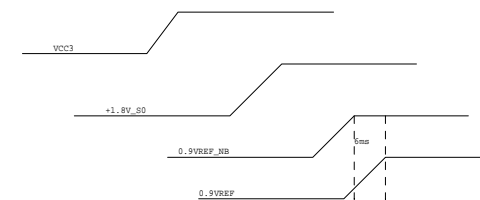
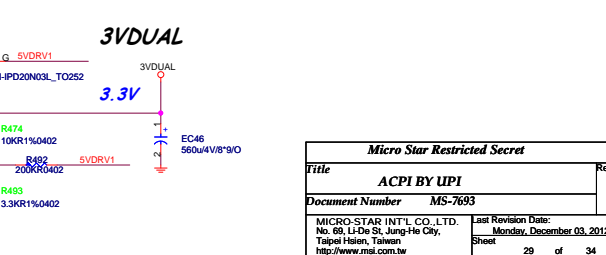
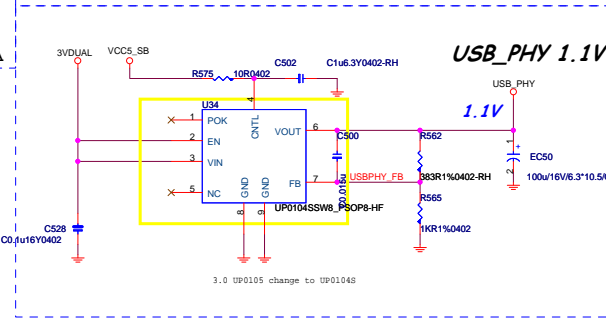
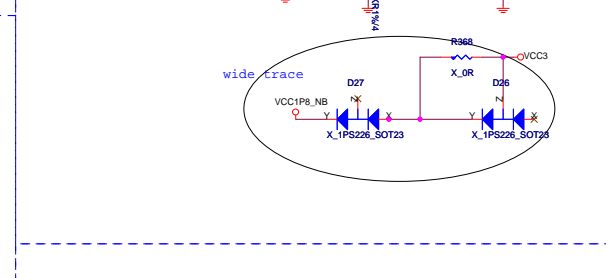


ESD Protection



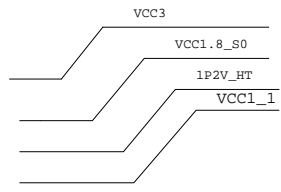
Important--
If USB3.0 signal connect to front pin header,
please must less than 2 inch, 1.5 inch is better.
USB3.0 test will fail in factory if you aren't follow this rule.

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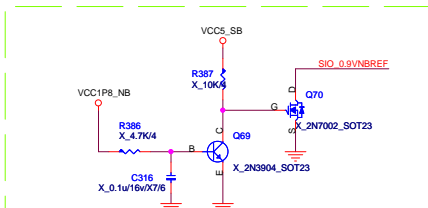
[illegible]

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Title	ACPI BY UPI	Rev
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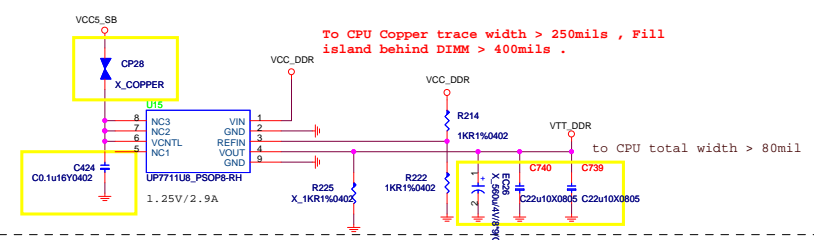
RX780 power up sequence



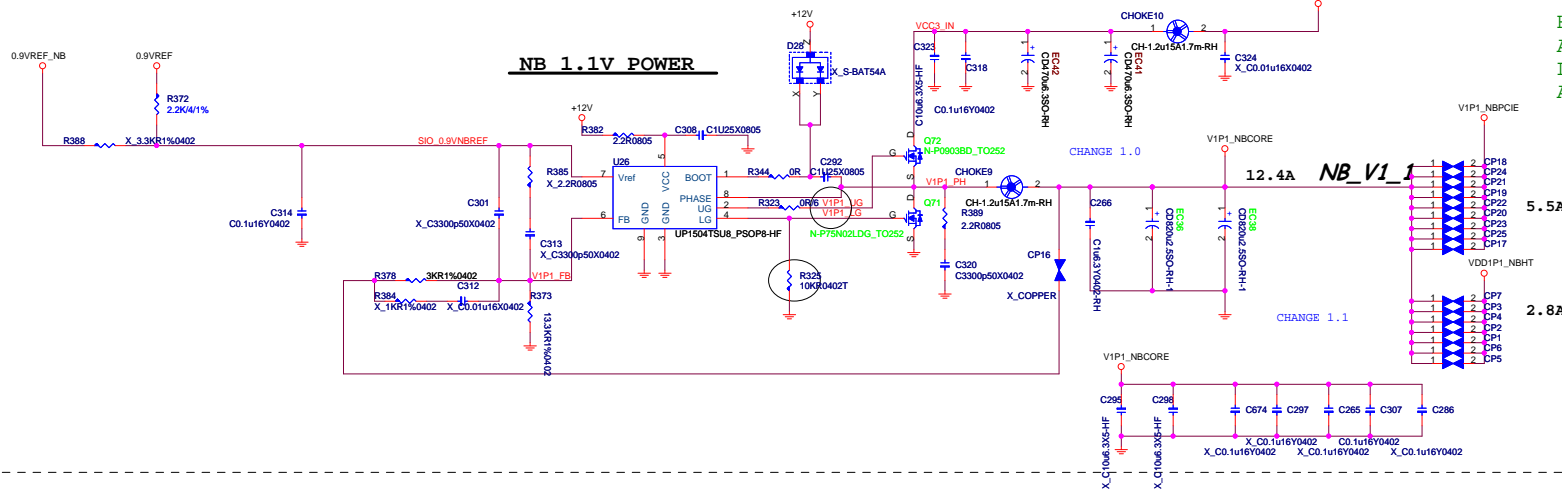
Reserve for RX980 POS



DDR VTT Power

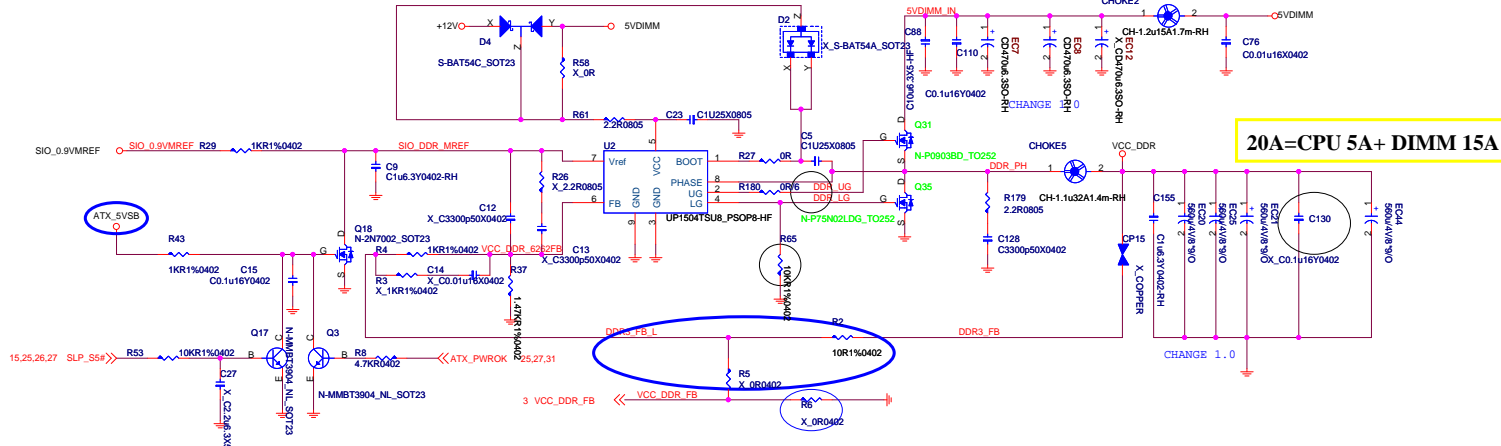


NB 1.1V POWER



H-MOS: D03-0903BDB-N03
AVL: D03-0480900-005
L-MOS: D03-75N022B-N03
AVL: D03-0480600-005

DDR III 1.5V POWER

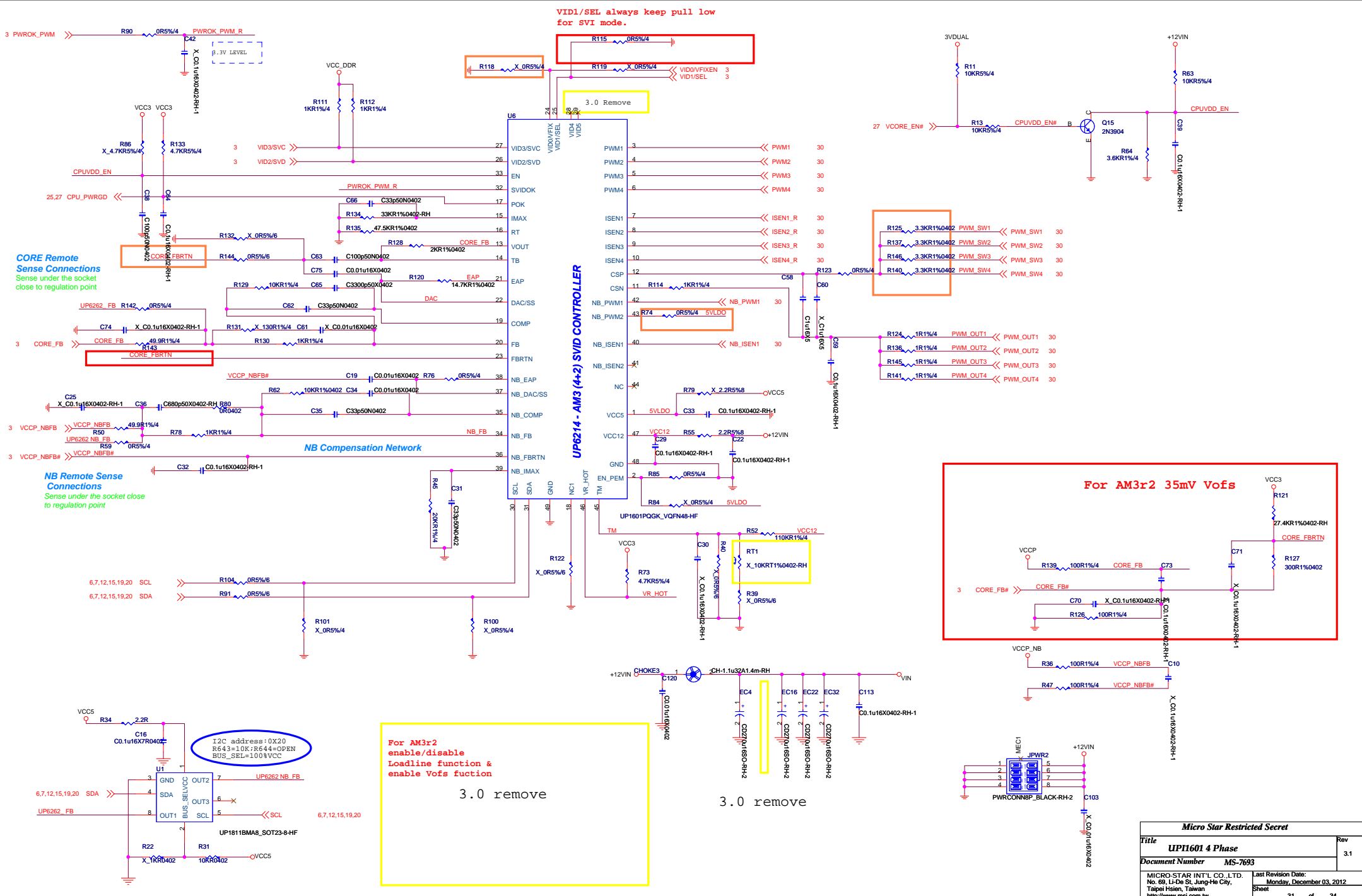


VCC_DDR

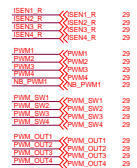
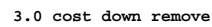
20A=CPU 5A+ DIMM 15A

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VCCP:110A VCC_NB:20A



Title WATER & WETLANDS, 1

VRM UPI6282 drive

Document Number	MS-769
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D.	Last Revision Date: Monday, December 03, 2012
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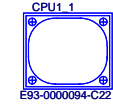
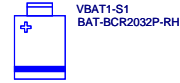
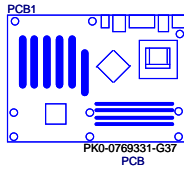
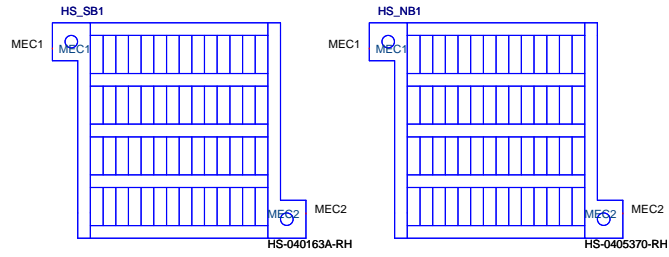
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Intel Front Panel

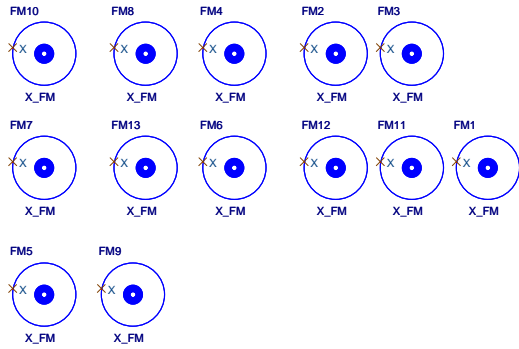


Title	Rev
ATX connector / Front Panel/KB	3.1
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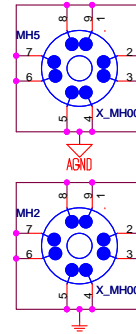
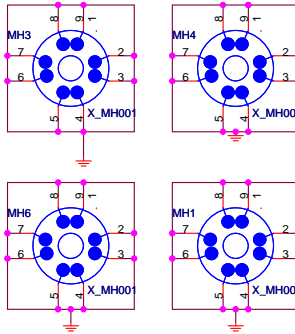
MK1
G51-M1SPD29-Q13



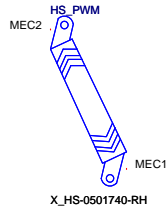
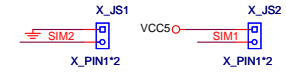
Optics Orientation Holes



Mounting Holes



Simulation



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